Design System for Locally Fabricated Gallium Arsenide Digital Integrated Circuits

by

Anthony Edward Parker

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

Monday, 26 November, 1990

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Gallium Arsenide Digital Integrated Circuits Project,
Laboratory for Communication Science and Engineering,
Sydney University Electrical Engineering.
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Abstract

In order to enable and encourage system designs in the area of Gallium Arsenide (GaAs) circuits, the Laboratory for Communication Science and Engineering at the University of Sydney and the CSIRO Division of Radiophysics have been collaborating to establish a local GaAs digital integrated design and fabrication capability. The aim of this project is to produce a digital GaAs technology compatible with the emerging analog technology so that it can be used in new applications. This thesis addresses both the development of the design techniques needed to produce custom GaAs logic circuits with the low noise fabrication process being developed at the CSIRO and the setting up of design and testing tools which provide circuit simulations, mask layout and assistance in circuit design. The output of this thesis is the forerunner to the establishment of a GaAs logic circuit design facility tailored to the anticipated local capability.

The developments reported in the thesis include: an improvement to the SPICE JFET model and an extension of the JFET model to accurately model MESFET’s, the development of an automatic system for designing basic logic gates which produces a ‘template’ BFL gate for the generation of a logic gate library, and the development of a switched-linear modelling technique which features the ability for automatic extraction of gate-level models. An understanding of the operation of the basic gate results in the development of a new high performance logic family.

The design system developed in this thesis is an automated link between the fabrication process and design tools. The equations developed allow the derivation of device model parameters for the various passive and active components from the basic physical and electrical properties of the material and devices. This first-principle approach was adopted so that the system can accommodate changes to materials, fabrication techniques and circuit devices. The design system has the long term benefit that it will allow the design facility to keep pace with technological development.
Acknowledgement

The author wishes to thank...

Professor David Skellern for his advice and encouragement as mentor and project supervisor.

Professor Trever Cole who supervised while David Skellern was on sabbatical and after he left Sydney University.

John Archer, Bob Batchelor, Grant Griffiths, Warren King and other members of the Solid-State Group at CSIRO Division of Radiophysics for helpful discussions and fabrication of devices and circuits.

James Thompson and Tim Rogers at Telecom Australia Research Laboratory for their generous co-operation and assistance with the use of their Voltage Contrast Microscope.

Janet, to whom this work is dedicated, for her support as wife and friend and for sharing the hardship and inconvenience of postgraduate research.

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Australian Commonwealth Postgraduate Research Award,

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Statement of Originality

The work described in this thesis was carried out at the Department of Electrical Engineering, University of Sydney between March 1986 and December 1989, under the supervision of Dr. David Skellern. Professor Trever Cole supervised after David Skellern left Sydney University in 1989.

Circuits developed for this thesis were fabricated at the Commonwealth Scientific and Industrial Research Organisation (CSIRO) Division of Radiophysics by staff of the Solid State Group.

The body of the thesis consists of eight chapters and six Appendix sections. An outline of the main achievements of the work for this thesis is given in Chapter 1.

The work of others is acknowledged and referenced in the body of this thesis, except in cases when the results are widely known. Otherwise, the work in this thesis was originated by the author. The following paragraphs state the portions of the work which are claimed as original contributions of the author.

Chapter 2 contains a summary of the work of others except for the discrete element subcircuit MESFET model which is suitable for implementation in early versions of SPICE and was devised by the author.

An accurate MESFET model based on a refinement of the existing SPICE JFET model is described in Chapter 3. The concept of including short channel effects in the long channel FET model was due to the author. The model equation derived in Appendix section 9.5 and the modification to the SPICE code in Appendix section 9.4 are the original work of the author.

The equations developed in Chapter 4 allow the derivation of device model parameters from the basic physical and electrical properties of the material and devices. These equations were derived through an analysis carried out by the author of the work of others. An comparison of previously published parasitic capacitance equations with an accepted first principle derivation was carried out by the author to give improved capacitance extraction equations. The proposed correction to accepted application of thermionic emission theory to Schottky diodes was due to the author.
The idea of using simple piecewise linear transistor models to analyse Buffered FET Logic (BFL) gate design was due to the author. This analysis was expanded by the author to give an automated procedure for designing a ‘template’ BFL gate as described in Chapter 5.

The idea of using switched-linear networks was proposed by David Skellern and the implementation and development of an automatic extraction process was carried out by the author. The development of a switched-linear network model is described in Chapter 6. Insight into the operation of the gate gained through this development revealed to the author that a minor modification to BFL gives increased performance. The resulting new logic family is described in Chapter 5. The gate-level implementation from an existing block diagram of the serial multiplier used to verify the models was carried out by the author.

The software package, GaAsSPICE, described in Chapter 7 was originally written by the author to determine SPICE model parameters and later expanded to incorporate the gate gate design procedure described in Chapter 5.

The material in this thesis has not been submitted towards another degree at this or any other university.
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List of Special Names and Symbols

**Abbreviations**

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<tr>
<th>Abbreviation</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>Aluminium</td>
</tr>
<tr>
<td>ANZAAS</td>
<td>Australian and New Zealand Association for the Advancement of Science</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>ATERB</td>
<td>Australian Telecommunications and Electronics Research Board</td>
</tr>
<tr>
<td>Au</td>
<td>Gold</td>
</tr>
<tr>
<td>AuGe</td>
<td>Gold Germanium</td>
</tr>
<tr>
<td>BFL</td>
<td>Buffered FET Logic</td>
</tr>
<tr>
<td>CCFL</td>
<td>Capacitor Coupled FET Logic</td>
</tr>
<tr>
<td>CDFL</td>
<td>Capacitor Diode FET Logic</td>
</tr>
<tr>
<td>Cr</td>
<td>Chrome</td>
</tr>
<tr>
<td>CSIRO</td>
<td>Commonwealth Scientific and Industrial Research Organisation</td>
</tr>
<tr>
<td>DCFL</td>
<td>Direct Coupled FET Logic</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter Coupled Logic</td>
</tr>
<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>InP</td>
<td>Indium Phosphide</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction Field-Effect Transistor</td>
</tr>
<tr>
<td>LSI</td>
<td>Large Scale Integration</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MODFET</td>
<td>Modulation Doped Field-Effect Transistor</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MSI</td>
<td>Medium Scale Integration</td>
</tr>
<tr>
<td>Ni</td>
<td>Nickel</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>Pd</td>
<td>Palladium</td>
</tr>
<tr>
<td>Pt</td>
<td>Platinum</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computer</td>
</tr>
<tr>
<td>SBFL</td>
<td>Saturated Buffer FET Logic</td>
</tr>
<tr>
<td>SCFL</td>
<td>Source Coupled FET Logic</td>
</tr>
<tr>
<td>SDFL</td>
<td>Schottky Diode FET Logic</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>SPICE</td>
<td>Simulation Program with Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>Ti</td>
<td>Titanium</td>
</tr>
<tr>
<td>TOM</td>
<td>TriQuint’s Own Model</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
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Physical Constants

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>Richardson constant</td>
<td>$1.2 \times 10^6$</td>
<td>A/m$^2$/K</td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>Permittivity of free space</td>
<td>$8.8541853 \times 10^{-12}$</td>
<td>F/m</td>
</tr>
<tr>
<td>$q$</td>
<td>Charge of an electron</td>
<td>$1.6021917 \times 10^{-19}$</td>
<td>C</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann constant</td>
<td>$1.380622 \times 10^{-23}$</td>
<td>J/K</td>
</tr>
<tr>
<td>$\pi$</td>
<td></td>
<td>$3.141592654$</td>
<td></td>
</tr>
</tbody>
</table>

Device Dimensions

Current flow is conventionally thought of as flowing along the length of a device which is very often much less than the dimension perpendicular to the current flow. Thus the device length is usually less than its width and leads to confusion because in common English usage the term length is applied to the larger dimension. In keeping with convention length is defined as the dimension parallel to the flow of current.

$l$ Length of feature parallel to flow of current.

$z$ Width of feature perpendicular to flow of current†.

$d$ Distance between features parallel to flow of current.

† The use of $z$ (rather than $w$) for width follows from its use by Shockley, van der Ziel, Pucel and others in their discussions of transistor behaviour.
Symbols

\begin{align*}
A & \quad \text{MESFET current equation coefficient} \\
& \quad \text{c.f.} A \text{ used for the Richardson constant} \\
a & \quad \text{FET channel thickness} \\
\alpha & \quad \text{MESFET saturation parameter} \\
A^* & \quad \text{Richardson constant corrected for electron mass} \\
& \quad A/m^2K^2 \\
B & \quad \text{MESFET doping profile parameter} \\
b & \quad \text{MESFET doping tail extending parameter} \\
\beta & \quad \text{Transconductance parameter in FET equations} \\
C & \quad \text{Capacitance} \\
c_1 & \quad \text{Surface state parameter for built-in potential} \\
c_2 & \quad \text{Surface state parameter for built-in potential} \\
C_C & \quad \text{Capacitance between coplanar strips} \\
C_{\text{dfb}} & \quad \text{Effective drain feedback capacitance} \\
C_{\text{dfbo}} & \quad \text{Drain feedback capacitance parameter} \\
C_{\text{gd}} & \quad \text{FET gate-drain junction capacitance} \\
C_{\text{gr}} & \quad \text{Parasitic capacitance to ground} \\
C_{\text{gs}} & \quad \text{FET zero-biased gate-source junction capacitance} \\
C_{\text{jo}} & \quad \text{Zero-biased junction capacitance} \\
\Delta & \quad \text{Width of capacitance drain-source reversal parm.} \\
\delta & \quad \text{-Width parameter of junction capacitance reduction} \\
& \quad \text{-TOM current reduction parameter} \\
d & \quad \text{Extent of FET channel depletion at drain end} \\
& \quad \text{c.f.} d \text{ used for distance between features} \\
d_d & \quad \text{Length of planar diode Schottky metal} \\
d_e & \quad \text{Length of epi-layer} \\
& \quad \text{between ohmic and Schottky metals} \\
d_o & \quad \text{Length of planar diode ohmic metal} \\
\Delta V_{\text{sfh}} & \quad \text{Effective voltage change of the gate-source junction} \\
& \quad \text{of source follower during a falling transition} \\
\Delta V_{\text{sfl}} & \quad \text{Effective voltage change of the gate-source junction} \\
& \quad \text{of source follower during a rising transition} \\
E & \quad \text{Electric field strength} \\
\varepsilon & \quad \text{Material permittivity} \\
E_b & \quad \text{Semiconductor breakdown field} \\
E_g & \quad \text{Electron energy bad gap} \\
E_m & \quad \text{Maximum electron velocity field} \\
\varepsilon_o & \quad \text{Permittivity of free space} \\
\varepsilon_r & \quad \text{Material permittivity relative to free space}
\end{align*}
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_s$</td>
<td>Effective electron velocity saturation field</td>
<td>V/m</td>
</tr>
<tr>
<td>$F$</td>
<td>Designed fan-out loading</td>
<td>-</td>
</tr>
<tr>
<td>$f$</td>
<td>-Frequency</td>
<td>Hz</td>
</tr>
<tr>
<td></td>
<td>-Actual fan-out loading</td>
<td>-</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>Diode barrier built-in potential</td>
<td>eV</td>
</tr>
<tr>
<td>$F_C$</td>
<td>Coefficient for forward-bias junction capacitance formula</td>
<td>-</td>
</tr>
<tr>
<td>$f_{in}$</td>
<td>Fan-in</td>
<td>-</td>
</tr>
<tr>
<td>$\phi_m$</td>
<td>Schottky metal work function</td>
<td>eV</td>
</tr>
<tr>
<td>$f_{out}$</td>
<td>Fan-out</td>
<td>-</td>
</tr>
<tr>
<td>$\Gamma$</td>
<td>MESFET current reduction coefficient</td>
<td>-</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>TriQuint MESFET model saturation parameter</td>
<td>-</td>
</tr>
<tr>
<td>$G_{ds}$</td>
<td>FET drain-source conductance</td>
<td>S</td>
</tr>
<tr>
<td>$g_m$</td>
<td>FET gate-source to drain-source transconductance</td>
<td>A/V</td>
</tr>
<tr>
<td>$G_s$</td>
<td>Conductance of saturation potential</td>
<td>S</td>
</tr>
<tr>
<td>$g_x$</td>
<td>Near-pinch-off transconductance</td>
<td>A/V</td>
</tr>
<tr>
<td>$\eta$</td>
<td>MESFET drain feedback parameter</td>
<td>-</td>
</tr>
<tr>
<td>$h_e$</td>
<td>Effective thickness of epi-layer</td>
<td>m</td>
</tr>
<tr>
<td>$I_{available}$</td>
<td>Available charging current</td>
<td>A</td>
</tr>
<tr>
<td>$I_d$</td>
<td>Reverse leakage current of second diode in planar model</td>
<td>-</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>FET drain to source current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{ds,s}$</td>
<td>Zero-gate-bias saturated drain current</td>
<td>A</td>
</tr>
<tr>
<td>$I_m$</td>
<td>Velocity limited maximum FET current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Maximum MESFET drain current</td>
<td>A</td>
</tr>
<tr>
<td>$I_s$</td>
<td>Diode reverse leakage current</td>
<td>A</td>
</tr>
<tr>
<td>$I_x$</td>
<td>Near-pinch-off zero-gate-bias saturated current</td>
<td>A</td>
</tr>
<tr>
<td>$J$</td>
<td>Current density</td>
<td>A/m²</td>
</tr>
<tr>
<td>$J_o$</td>
<td>Diode reverse leakage current density</td>
<td>A/m²</td>
</tr>
<tr>
<td>$k$</td>
<td>Geometry parameter in capacitance formula</td>
<td>-</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>MESFET drain current reduction parameter</td>
<td>-</td>
</tr>
<tr>
<td>$l$</td>
<td>Length of feature parallel to flow of current</td>
<td>m</td>
</tr>
<tr>
<td>$L$</td>
<td>Length of FET gate</td>
<td>m</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>FET channel-length modulation parameter</td>
<td>1/V</td>
</tr>
<tr>
<td>$l_1$</td>
<td>Length of unsaturated region of FET</td>
<td>m</td>
</tr>
<tr>
<td>$L_o$</td>
<td>Drain feedback gate length parameter</td>
<td>F</td>
</tr>
<tr>
<td>$L_{sat}$</td>
<td>Length of saturated region of MESFET channel</td>
<td>m</td>
</tr>
</tbody>
</table>
\( L_t \) Ohmic contact transfer length \( \text{m} \)

\( \mu \) Low field electron mobility \( \text{m}^2/\text{V} \cdot \text{s} \)

\( m^*/m \) Relative mass of electrons in semiconductor

\( m_{m}/m \) Relative mass of electrons in Schottky metal

\( N \) Diode junction ideality factor

\( n \) Exponent in general power-law equation

\( N_c \) Density of conduction states in valence band of semiconductor \( \text{m}^{-3} \)

\( N_{co} \) Density of conduction states in valence band of semiconductor at 300 K \( \text{m}^{-3} \)

\( N_d \) Nominal doping level of semiconductor \( \text{m}^{-3} \)

\( p \) Extent of FET channel depletion at saturation point

\( Q \) Electric charge \( \text{C} \)

\( \theta \) MESFET drain current reduction Parameter

\( Q_{ss} \) Total charge under FET gate \( \text{C} \)

\( R \) Resistance \( \Omega \)

\( R_a \) Ohmic contact alloy sheet resistance \( \Omega \cdot \text{sq} \)

\( R_c \) Contact metal-alloy interface resistance \( \Omega \cdot \text{m}^{-2} \)

\( R_{dd} \) MESFET drain electrode parasitic resistance \( \Omega \)

\( R_s \) Semiconductor sheet resistance \( \Omega \cdot \text{sq} \)

\( R_{ss} \) MESFET source electrode parasitic resistance \( \Omega \)

\( s \) Extent of FET channel depletion at source end

\( T \) Operating temperature \( \text{K} \)

\( \tau \) Time constant for high frequency drain feedback \( \text{s} \)

\( t \) Time \( \text{s} \)

\( \tau_f \) Fall-time \( \text{s} \)

\( \tau_r \) Rise-time \( \text{s} \)

\( \tau_t \) Transit-time \( \text{s} \)

\( V \) Electric potential \( \text{V} \)

\( v \) Electron velocity \( \text{m/s} \)

\( V_b \) Diode junction breakdown potential \( \text{V} \)

\( V_d \) Potential across level-shift diode chain \( \text{V} \)

\( v_D \) Drift velocity of electrons in semiconductor \( \text{m/s} \)

\( V_{dd} \) Positive power supply potential \( \text{V} \)

\( V_{ds} \) FET drain-source potential \( \text{V} \)

\( V_{ds \, pd} \) Drain-source potential of pull-down transistor \( \text{V} \)
\( V_{ds\,pu} \) Drain-source potential of pull-up transistor \( V \)

\( V_{ds\,sf} \) Drain-source potential of source follower \( V \)

\( V_{ds\,sw} \) Drain-source potential of switch transistor \( V \)

\( V_g \) Potential above pinch-off of FET gate-source bias \( V \)

\( V_{gd} \) FET gate-drain potential \( V \)

\( V_{gs} \) FET gate-source potential \( V \)

\( V_h \) Logic high potential \( V \)

\( V_l \) Logic low potential \( V \)

\( V_{lower} \) Threshold logic level of lower gate of dual-gate transistor \( V \)

\( u_m \) Maximum electron velocity \( m/s \)

\( V_{mid} \) Threshold logic level \( V \)

\( V_p \) FET channel potential at saturation point \( V \)

\( V_{po} \) Effective MESFET pinch-off potential \( V \)

\( V_r \) Effective trap potential in MESFET \( V \)

\( u_R \) Velocity of electrons crossing Schottky Barrier \( m/s \)

\( V_s \) Effective zero-current saturation potential \( V \)

\( u_s \) Saturated electron velocity \( m/s \)

\( V_{sat} \) FET drain-source saturation potential \( V \)

\( V_{ss} \) Negative power supply potential \( V \)

\( V_{to} \) FET pinch-off or diode depletion potential \( V \)

\( V_{upper} \) Threshold logic level of upper gate of dual-gate transistor \( V \)

\( \omega \) Angular frequency \( \text{rad/s} \)

\( W_{oo} \) Total potential required to deplete FET channel \( V \)

\( \xi \) FET saturation index \( - \)

\( X_C \) Pinch-off coefficient for junction capacitance formula \( - \)

\( \zeta \) MESFET high frequency drain feedback parameter \( - \)

\( z \) Width of feature perpendicular to flow of current \( m \)

\( z_{an} \) Width of dual gate transistor \( m \)

\( z_{pd} \) Width of pull-down transistor \( m \)

\( z_{pu} \) Width of pull-up transistor \( m \)

\( z_{sf} \) Width of source follower \( m \)

\( z_{sw} \) Width of switch transistor \( m \)
1 Introduction

Since the first investigation of Gallium Arsenide (GaAs) transistors in the early 1970’s, the development of GaAs devices has brought about unequalled gain, noise performance and bandwidth in analog microwave circuits and unequalled switching rates in digital applications. As a result, GaAs integrated circuits are found increasingly in very high performance systems in communications, computers and instrumentation. Gallium Arsenide also permits an increase in the performance of these systems which otherwise would have been impossible or impractical using silicon semiconductors. For example, future communications standards including high speed trunks together with local area and subscriber networks capable of carrying coded video; information to each subscriber will require high data rates offered by GaAs technology.

Many applications require a combination of analog and digital functions in order to meet their performance requirements. Digital signal processors require analog to digital conversion before the signal can be processed and optical links require optical as well as analog and digital functions. Ideally, digital and analog functions should be integrated on a single die.

The integration of digital circuits with analog circuits requires the development of a digital technology using low-noise analog fabrication techniques. This imposes limitations on the type of useful circuits that can be fabricated. However, this presents a niche in the world market which can be filled by an Australian GaAs facility with the requisite capability and an aim of this thesis has been to provide the necessary knowledge base and tools to enable industry to seize the opportunity. The challenges faced in this development include adapting to the fabrication technique and satisfying the need for computer tools which enable rapid design and verification.

This thesis provides the basic tools required to establish a digital logic circuit design facility tailored to a low noise MBE based GaAs capability. Circuit simulation
models and design and layout tools necessary for the implementation of GaAs digital logic are presented. These have been developed for use with a basic analog fabrication process but are oriented towards easy adaptation as process techniques improve.

This introduction describes Gallium Arsenide and its advantages and gives a brief outline of GaAs applications and the scope for combined analog and digital integration. The development of a capability in the area of combined digital and analog applications is identified as the aim for the project. An outline of the scope of this thesis, the requirements for its development and the approach adopted are given. Finally, there is a synopsis which outlines the content of the following chapters.

1.1 Gallium Arsenide Technology

GaAs devices have become established in analog microwave applications because of their superior gain and noise performance. For digital applications Gallium Arsenide offers an increased speed-power product that permits the development of very high speed systems in communications, computers and instrumentation. Review papers on GaAs digital applications provide an extensive source of information from which a brief summary is presented in this section. Good reviews of GaAs technology are given by Eden et al. [1983] and Eden [1988]. The material characteristics of GaAs and its advantages are discussed by Nuzillat et al. [1982] and an outline of how high electron mobility in GaAs improves high speed performance is given by Eden [1982a].

1.1.1 Characteristics of GaAs

The Gallium Arsenide III-V compound forms a homogeneous crystal with an electron bonding structure similar to silicon. However, it has a different energy band structure which provides three main advantages. Firstly, the electron mobility is higher so for microwave analog work GaAs offers lower noise and power consumption than silicon and in digital applications a higher operating speed is achievable. GaAs ring oscillator propagation delays as low as 30 ps are ten times faster than 300-400 ps delays for Si bipolar and MOS technologies [Greiling 1985] and over six times faster than 200-300 ps for ECL gate arrays [Eden 1982b]. Secondly, GaAs electron band-gap energy is larger which results in improved electron security. This provides a natural semi-insulating substrate which allows the fabrication of epitaxial active layers directly on wafers. Also for military and space applications, GaAs integrated circuits offer exceptional radiation hardness ($10^7$ to $10^8$ rd) [Zuleeg 1989]. For automotive or geological
applications, GaAs can work in wide temperature ranges between $-200^\circ$C and $+200^\circ$C [Eden et al. 1983]. Thirdly, like most III-V compounds, the band-gap transitions are direct and result in the emission of photons. Thus GaAs offers optical devices for high speed sources and detectors.

There are disadvantages. Fabrication is complicated because the crystal is brittle, there is no native oxide for the creation of insulating layers, and very small sub-micron dimensions (0.5 to 1.0 $\mu$m gate lengths) are required. Also, the mobility of holes is very low so for high speed applications the technology is restricted to n-type devices. The adoption of GaAs requires a re-think in system architecture so that the design can take full advantage of the technology. The trade-offs involved are discussed by Gilbert [1984] and the issues involved in designing high speed data paths and architectures by Gilbert et al. [1986].

Despite the drawbacks, manufacture in large quantities can be readily achieved and the speed and performance advantages often outweigh the disadvantages. A comparison with silicon circuits [Greiling 1985] shows at least a doubling in operation speed for multiplier circuits and half the power dissipation in memory applications. A comparison of GaAs propagation delay and power dissipation with that of other technologies is shown in Fig. 1.1 [Long et al. 1982, Eden et al. 1978, Mizutani et al. 1980a].

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† The temperature range is limited by use of gold based metals which undergo an alloying process at relatively low temperatures. Operation up to 400$^\circ$C should be possible with improved fabrication.
1.1.2 Applications for GaAs

Initial experiments with Gallium Arsenide in the 1960's were discouraging but the turning point came with the development of the MEtal Semiconductor FET (MESFET) in 1970 [Drangeid et al. 1970]. Over the decade after this development GaAs devices equalled and then exceeded the performance of silicon [Eden et al. 1978]. Digital circuits also took advantage of the high switching speed of MESFET devices and by the end of the decade following the development of the MESFET ring oscillator propagation delays as low as 30 ps/gate at room temp and 17.5 ps/gate at 77 K were reported [Mizutani et al. 1980b]. Delays between 60 and 100 ps/gate are usual in complicated circuits such as binary dividers. A list of some of the reported circuits is given in Table 1.1.

Initial development was with a mesa isolation process from which a reliable Buffered FET Logic (BFL) emerged [van Tuyl and Liechti 1974]. Planar fabrication using ion implantation techniques was later developed to increase yield and circuit complexity [Eden et al. 1978]. This achieved high density gate structures with uniform device characteristics and provided high speed logic with modest power dissipation (< 1 mW/gate). Increased interest in further refinement towards LSI and even VLSI has allowed the development of computer and memory circuits [Naused and Gilbert 1987, Hirayama et al. 1986, Milutinovic et al. 1986].

There is now much international interest in GaAs circuits which has resulted in a competitive, though not fully developed, industry with several foundry services capable of fabricating analog and digital MSI circuits. The three main foundries are GigaBit Logic who offer a standard library and an ‘application specific’ service up to 15,000 gates using Source Coupled Logic [1989 GigaBit Logic Data Book], Vitesse Semiconductor who specialise in large 17,000 gate gate-arrays, and TriQuint Semiconductor who offer monolithic microwave circuits and ‘application specific’ linear and digital IC’s with complexities up to 10,000 gates [Davis 1989]. The services provided by the foundries allow the production either of digital or of analog circuits but not the integration of digital and analog on a single die.

Applications for Combined Analog and Digital Integration

New applications involving high bandwidth signal processing are emerging and digital GaAs integrated circuits will be of primary importance. For example, GaAs will be required for high sample-rate digital filters [Gilbert 1984]. Existing MOS signal processors, such as switched capacitor systems, are restricted to approximately 15 MHz whereas GaAs systems can extend this to 100 MHz or more [Larson et al. 1987]. The
impact of GaAs circuits on gigabit rate signal processing is further discussed by Greiling [1985].

The application of GaAs in many new areas benefits from the integration of both analog and digital functions on the one chip in order to achieve the necessary speed without circuit interconnection bottle-necks. There are relatively small circuits such as 6 bit ‘flash’ analog-to-digital converters, frequency dividers and synthesizers which can be easily accommodated with an analog circuit [Podell 1983]. The application of digital filters in satellite links requires an analog input and analog-to-digital conversion before the signal can be processed. Another example is an optical link which requires analog handling of the optical information before the digital processing. Although GaAs does not provide the optimum optical wavelengths for fibre systems, it serves as a gateway for developments in other materials [Shibata and Kajiwara 1989].

As the push to even higher data rates continues, combined analog and digital integration will need even faster devices. A device which shows promise in the analog area is the High Electron Mobility Transistor (HEMT) which offers higher speed and better noise performance than the conventional GaAs transistor. An excellent overview on this device is given by Drummond et al. [1986].

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1966</td>
<td>Fabrication of first MESFET</td>
<td>Mead 1966</td>
</tr>
<tr>
<td>1970</td>
<td>Development of the MESFET in GaAs</td>
<td>Drangeid et al. 1970</td>
</tr>
<tr>
<td>1974</td>
<td>Development of BFL with 100 ps delay</td>
<td>van Tuyl and Liechti 1974</td>
</tr>
<tr>
<td>1976</td>
<td>Discrete microwave GaAs transistors</td>
<td>Long et al. 1980</td>
</tr>
<tr>
<td>1978</td>
<td>Development of Planar GaAs technology</td>
<td>Eden et al. 1978</td>
</tr>
<tr>
<td>1979</td>
<td>MSI with 75 SDFL gates 75-200 ps delays</td>
<td>Long et al. 1980</td>
</tr>
<tr>
<td>1980</td>
<td>GaAs MOSFET logic 110 ps ring oscillator</td>
<td>Yokoyama et al. 1980</td>
</tr>
<tr>
<td>1981</td>
<td>2.1 ns 4 Bit Arithmetic Logic Unit</td>
<td>Suyama et al. 1982</td>
</tr>
<tr>
<td>1982</td>
<td>18.4 ps HEMT ring oscillator</td>
<td>Morkoç and Solomon 1984</td>
</tr>
<tr>
<td>1984</td>
<td>4 Kbit Static Ram (2.6 ns)</td>
<td>Mizoguchi et al. 1984</td>
</tr>
<tr>
<td>1984</td>
<td>2 K Gate Array</td>
<td>Peczalski et al. 1986</td>
</tr>
<tr>
<td>1984</td>
<td>4 × 4 GaAs Multiplier (2.5 ns)</td>
<td>Delhaye et al. 1987</td>
</tr>
<tr>
<td>1987</td>
<td>13.5 GHz Frequency Divider</td>
<td>Osaafune and Ohwada 1987</td>
</tr>
<tr>
<td>1987</td>
<td>200 MHz 32 Bit GaAs RISC Processor</td>
<td>Naused and Gilbert 1987</td>
</tr>
<tr>
<td>1987</td>
<td>100 MHz Switched Capacitor Signal Processor / 920 MHz Op-Amp</td>
<td>Larson et al. 1987</td>
</tr>
<tr>
<td>1988</td>
<td>HEMT 25 GHz static divider</td>
<td>Jensen et al. 1988</td>
</tr>
</tbody>
</table>
1.2 Aim of Project

A challenge taken up in Australia is to establish a firm position in the world market in high performance areas of information technology which require low noise microwave analog and digital integration. In order to encourage system designs in this field, the Laboratory for Communications Science and Engineering at the University of Sydney and the CSIRO Division of Radiophysics have been collaborating to establish a local GaAs digital integrated design and fabrication capability. The Division of Radiophysics has a GaAs laboratory for developing analog microwave devices including the HEMT. The project’s aim is to produce a digital GaAs technology compatible with this emerging analog technology. Although the long term goal is to have a digital capability suitable for integration with the emerging HEMT technology, developments in the first years were with MESFET devices. The collaboration proceeded in three areas:

**Development of Custom GaAs Techniques**

The first step in the collaboration was the development of design, fabrication, packaging and testing techniques needed to produce custom GaAs logic circuits. This required the development of techniques applicable to a low noise analog fabrication process. The development of the HEMT was the long term goal which requires an accurately layered crystal wafer produced by a Molecular Beam Epitaxy (MBE) process. Initially this was not available so Schottky barrier diodes and depletion mode MESFET’s were used. A mesa isolation process was used for circuit fabrication because it is necessary for HEMT devices. The active devices are separated on the wafer by etching away the regions between them. The problem for digital circuits is that the density of the circuit is limited by the mesa structure which occupies more area than the planar technologies used by overseas foundries in ‘digital only’ circuits. Also, the use of only depletion mode MESFET’s imposes limitations on the type of circuit that can be made. The present state-of-the-art in mesa based GaAs digital circuits is larger and more power hungry than its silicon equivalent. Although the speed advantage still outweighs the disadvantages it was desirable to ameliorate them. The development of enhancement mode devices would offer much improved integration capability but these are difficult to fabricate.

**Establishment of a GaAs Design Facility**

Design and testing tools for circuit simulations and mask layout were established
in parallel with the development of GaAs technique. This involved the setting up and acquisition of expertise in computer based tools. These form part of a GaAs logic circuit design facility with skills accessible to industry.

**Education**

The early introduction of educational courses at the University of Sydney is important for establishing a base of design engineers able to use GaAs technology. GaAs integrated circuit design courses have been run and further courses, including an intensive industry-oriented course, are planned.

### 1.3 Scope of this Thesis

This thesis addresses both the development of the design techniques needed to produce custom GaAs logic circuits with the low noise fabrication process being developed at the CSIRO and the setting up of design and testing tools for circuit simulations and mask layout. This is the forerunner to the establishment of a GaAs logic circuit design facility.

#### 1.3.1 Requirements

The design facility required a set of rules for using the fabrication process and computer tools for assembling and designing circuits. These need to be accurate for both analog and digital applications and must at a later stage be able to accommodate enhancement mode or HEMT technologies. A set of basic logic gates must be developed so that complex circuits can be fabricated successfully using software layout tools to assemble the standard cells.

There are three areas which required development:

**Modelling**

Fundamental to the design of modern integrated circuits is a means to simulate circuit behaviour on a computer. The modelling system should be efficient enough for practical economic use but have sufficient accuracy and flexibility so that both analog and digital systems can be studied.

A single modelling tool cannot provide these for every application so the modelling system has levels applicable to the different jobs at hand. At the first level, a detailed
and accurate model is required as a ‘bench-mark’ reference. The second level is a circuit model suited to computer simulation of single devices or logic gates. The third level is a simple but accurate model suited to simulation of a complete system.

**Circuit Design**

A design procedure, preferably automatic, is required so that logic circuit designs which satisfy power and speed requirements can be rapidly carried out. Basic building blocks of logic function families with various power capabilities are required. These sub-assemblies can then be combined to form complete systems.

**Design Rules**

A reliable set of design rules for circuit layout which consider limitations of lithography, mask alignment, processing and electrical design is required. The limiting consideration was lithography which restricted the minimum feature size to 1.5 microns. Sub-micron features which call for electron beam lithography were planned for 1990 to allow production of faster circuits.

**1.3.2 Approach Adopted**

The programme of research for this thesis has been heavily influenced by limitations on the availability of resources and experimental data.

Much of the development needed to concentrate on the creation of suitable device models with accuracy in both analog and digital applications. Although several MESFET models do exist, they are either far too complicated for practical computer simulators or have been developed as good models for standard devices and do not allow the exploration of extreme device behaviour and operation.

A fundamental approach was adopted so that device models could be derived reliably without measuring large numbers of transistor characteristics. As a result the models developed use parameters which can be related to a specific physical phenomena of device operation. Approximate descriptions are used within the circuit models to maintain computational efficiency. Parameters are made available for independent adjustment of each identifiable phenomenon. Where practical, physical descriptions of the phenomena are used directly in the derivation of these parameters. In other cases they are derived with empirical expressions.
As it transpired, the fundamental approach was useful because the fabrication
capability was developing in parallel with the development of the digital design capabil-
ity. The approach provided three main advantages. Firstly, a change in the fabrication
process can be accommodated by re-applying the developed fundamental procedures.
Secondly, it is adaptable to a fundamental change such as a change of material, from
GaAs to InP for example, or a move from MESFET to HEMT technology. Thirdly, when
the system is automated, it can serve as tool for the appraisal of fabrication changes.

The SPICE circuit simulator available at the beginning of the work did not include
any form of MESFET model so initial work was carried out with complicated subcircuits.
The development of a new MESFET model was later possible with version 3b1 of SPICE
because the models are easily modified. However, as the current status of this program
does not support temperature analysis, different model parameters must be used for
simulations at different temperature. This is not a disadvantage as it is still necessary
to use several sets of model parameters to account for extremes due to fabrication
variance.

The main interface to the design system is PC based to give an inexpensive tool
which is readily available to industries contemplating development in GaAs. This also
provided a front-end which is very easy to modify as the system developed.

1.4 Synopsis

The outline of this thesis is as follows.

Chapter 1 has outlined the motivation for this work which has been reported in
two interim review papers. These are reproduced in Appendix section 9.2 and give a
description of the goal of the research project of which this thesis is a part.

A. E. Parker, “Gallium Arsenide Integrated Circuits”, Presented at Australian and New Zealand
Association for the Advancement of Science (ANZAAS) Centenary Congress, University of
Sydney, Very Large Scale Integrated Circuits Section, 16-20 May 1988.

Performance of Locally Fabricated GaAs Digital IC’s”, Microelectronics Conference VLSI 1987,

Chapter 2 contains a summary of the present state of GaAs technology which is
necessary background for the subsequent chapters. Included are the basic material and
electron transport properties, fabrication techniques, available devices including their
operation and current modelling techniques and the various types of digital logic. Also
included in the chapter is a discrete element subcircuit suitable for implementing a simple MESFET model with early versions of SPICE. This was developed as part of the research for this thesis but later superseded.

Chapter 3 presents a solution to the problem of modelling MESFET's with the SPICE simulation program. A unique and accurate MESFET model is developed based on a refinement of the existing SPICE JFET model. GaAs integrated digital and analog circuits need short gate lengths and this introduces high electric fields and ballistic effects which have been included in the model. This is especially important if the model is to be good for analog as well as digital circuits. The refinement of the existing SPICE JFET model is discussed in


Chapter 4 discusses the extraction of device model parameters for the various passive and active components. The equations developed in this chapter allow the derivation of device model parameters from the basic physical and electrical properties of the material and devices. Passive components are considered and an improved parasitic capacitance extraction technique is developed. The operation of the Schottky diode is carefully examined and a correction to accepted diode operation theory is applied for determining diode model parameters. Early work on the extraction process presented here is reported in


Chapter 5 develops a technique for designing basic digital logic gates. Simple models give an accurate and automated procedure for designing a ‘template’ BFL gate which is used for the generation of a complete logic gate library. Insight into the operation of the gate results in the development of a new high performance logic family and the performance of this family is discussed. This work forms the core of a software package developed in this project:

Chapter 6 develops the process of extracting simple switched-linear network models for rapid gate-level simulation. This is a particularly fruitful exercise as it provides a very accurate modelling technique which can be automatically derived. The technique for extracting these models is reported in


Chapter 7 explores the development of a design system which is an automated link between the fabrication process and design tools. A brief description and experimental verification is given. This brings together procedures developed in the previous chapters to form a design system reported in


Chapter 8 concludes the thesis with a summary of the work and a discussion of recommended future research. One area for development is analog design and an example of the use of the design system is reported in

1.4.1 Chapter 1 References


R. C. Eden, “Introduction to special issue on very fast solid-state technology”, *Proc. IEE*, vol. 70, no. 1, pp. 2-4, January 1982b.


2 Background
- GaAs, the Process, Device Physics, and Digital Logic

This chapter is a brief overview of GaAs technology, device modelling and digital logic schemes. It is not a complete outline of current GaAs technology but a selection which forms a basis for the subsequent chapters of the thesis. The discussion is divided into four areas. The first area is the basic material and electron transport properties of GaAs which give rise to advantages and disadvantages in the technology. It is necessary to collate these properties so that their influence on circuits can be considered and a brief list of properties and accepted descriptions for each is given here. The second area is the fabrication process which also must be understood in order to optimise circuit designs within the constraints imposed by the process. An outline of the process used by the CSIRO is presented. The third area is the identification of the types of electrical devices available and how to model their behaviour. In particular, the operation of and current modelling techniques for diodes and MESFET’s are considered. Finally, the fourth area of interest is the various implementations of digital logic.

The next section covers the first area by giving a brief description and some mathematical detail of the important electrical properties of GaAs.

2.1 Fundamental Properties of GaAs

There have been many review papers which outline the properties of the material and their influence on devices and fabrication processes. For example, material and device characteristics are discussed by Nuzillat et al. [1982] and Eden et al. [1982] and an historical overview is given by Eden [1988]. Textbooks covering GaAs devices are also available including the works by Shur [1987a], Sze [1985], Mun [1988], and van der Ziel [1976].
The Gallium Arsenide III-V compound forms a zincblende structure where the five valence electrons from each arsenic atom and the three from each gallium atom are shared homogeneously in the crystal. The crystal forms a brittle wafer with low thermal conductivity which complicates the design and fabrication process. Also, there is no native oxide suitable for applying the electrical insulation techniques developed for silicon IC’s. However, there are electrical advantages that make it worthwhile overcoming these obstacles.

Table 2.1 lists some of the major characteristics of both silicon and GaAs. These figures have been collated from several sources which give differing values. This arises because measured parameters, especially permittivity and mobility, are dependent upon the measuring apparatus and it is only as measurement techniques improve that better values are derived. Thus a chronological pattern can be found where the latest quoted value is most accurate.

### 2.1.1 Basic Electrical Properties

#### Band-Gap Energy

The electron bonding structure of GaAs is similar to that of silicon and germanium except that a different energy band structure exists. Three fundamental differences compared with silicon are that the band-gap is direct, the band-gap is larger and the effective electron mass is much lower. These differences affect the basic electron transport property of mobility and hence the operation of circuits.
The band-gap energy is temperature dependent as given by the empirical expression [Casey and Panish 1978, Sze 1985]:

\[ E_g = 1.519 - \frac{5.405 \times 10^{-4} T^2}{T^2 + 204} \text{[eV]} \]  
(2-1)

**Electron Mobility**

The most significant property of GaAs is the high electron mobility due to much lower effective electron mass in the crystal. A direct result is higher electron velocity so GaAs circuits are faster than their silicon counterparts and the power consumption is reduced because the same currents can be achieved with lower potentials than with silicon. For microwave analog work the increased mobility results in lower noise devices because the same power can be achieved with fewer scattering events than in silicon.

The mobility of holes, on the other hand, is very small (250 cm\(^2\)/V/s [Sze 1985]) so for high speed applications the technology is restricted to n-type devices.

A reduction in electron velocity occurs at high electric fields because the energy band structure of the crystal has a high energy valley in which electrons have a much larger effective mass (1.2 c.f. 0.067 in the lower valley). As electrons gain more energy in high electric fields, they occupy the high valley and their heavier effective mass reduces their velocity. In order to describe this phenomenon, an empirical description of velocity as a function of electric field is often used [Mizoguchi et al. 1984]:

\[ v(E) = \frac{\mu E + v_s (E/E_s)^4}{1 + (E/E_s)^4} \]  
(2-2)

However, different techniques of measuring the electron velocity are in considerable disagreement as shown by Ruch and Kino [1968]. This suggests that there are several factors which influence electron transport including the physical geometry of the conduction path. Dependence upon low field mobility, which in turn is dependent upon temperature and impurity levels, has been expressed by Shur [1987b] with the following comprehensive empirical description of electron velocity:

\[ v(E) = v_s \left[ 1 + \frac{E/E_s - 1}{1 + A(E/E_s)^t} \right] \]  
(2-3a)

\[ A = 0.6 \left[ e^{10(\mu - 0.2)} + e^{-35(\mu - 0.2)} \right]^{-1} + 0.01 \]  
(2-3b)

\[ t = 4 \left[ 1 + 320/sinh(40\mu) \right] \]  
(2-3c)
The drift velocity at low electric field is proportional to electric field strength and decreases with higher impurity concentration because of scattering effects. A good empirical fit to experimental data of Hilsum and Rose-Innes [1961] developed by the author for doping concentrations between $10^{15}$ and $10^{19}$ cm$^{-3}$ is

$$\mu = 5.81 \times 10^4 T^{-0.151} N_d^{0.151}$$  \[2-6\]

The drift velocity at low electric field is proportional to electric field strength and decreases with higher impurity concentration because of scattering effects. A good empirical fit to experimental data of Hilsum and Rose-Innes [1961] developed by the author for doping concentrations between $10^{15}$ and $10^{19}$ cm$^{-3}$ is

$$E_s = \frac{v_s}{\mu}$$  \[2-4\]
$$v_s = 10^5 (0.6 + 0.6\mu - 0.2\mu^2) \text{ [m/s]}$$  \[2-5\]

Resistivity

The resistivity of the intrinsic GaAs crystal is typically four orders of magnitude higher than that of silicon. This provides a fabrication advantage because the intrinsic material can be used as an insulating substrate with an active epitaxial layer grown directly on it. On the other hand, the thermal resistivity is also high and this limits the power dissipation and size of circuits. Packaging requires careful consideration of thermal limits.

Barrier Potential

There is no native oxide for creating MOS type enhancement mode transistors in GaAs. A high diode barrier that allows a significant forward bias is necessary for enhancement FET devices. GaAs diode junctions have a larger barrier potential than silicon junctions and this allows a 0.5 volt operating range.

Figure 2.1. Electron velocity in gallium arsenide as a function of electric field for various doping and temperature conditions.
Another property important for the calculation of diode barrier height is the density of conduction states which follows a three halves power of temperature [Sze 1985]:

\[ N_c = N_{co} \left( \frac{T}{300} \right)^{3/2} \]  

\[(2-7)\]

**Temperature and Radiation Hardness**

A large electron band-gap energy requires higher energy to move electrons into the conduction band which improves temperature stability and radiation hardness. With suitable fabrication GaAs circuits can work in wide temperature ranges between −200°C and +400°C. Thus it is an excellent choice for military, space, automotive and geological applications.

**Optical Property**

Like most III-V compounds, a direct band-gap transition in GaAs results in emission of photons. Therefore a major application for these compounds is optical devices for high speed sources and detectors. It should be pointed out that the wavelength of GaAs transitions is not ideal for current optical fibre use in the 1.3 - 1.5 μm range and other compounds such as InP are used. However, the use of InP for digital and analog circuits is in its infancy and most work is continuing with the better known GaAs material. Much of the design expertise in GaAs will be transferable to InP.

**2.1.2 Surface States**

Surface states have a significant influence on surface resistance, rectifying junctions and ohmic contacts, as discussed by Sze [1985]. Surface states arise from two sources.

Firstly, the general theories of quantum mechanics for a crystal structure assume that the crystal is infinite. It is with this assumption that the electron energy band structure and electrical properties are calculated. At the surface the crystal is bounded and the infinite structure description is not valid. However, the surface can be described with the infinite structure theory by including extra energy states. These states usually lie in the band-gap and are occupied by the surface electrons which would otherwise form bonds if the crystal was infinite. The excess electrons are said to be part of ‘dangling bonds’.

The second source of surface states arises from impurities and surface contamina-
tion which change the electron band structure at the surface. Unlike dangling bond states, surface contamination is not easily predicted and the fabrication process is usually refined to minimise it.

Surface states cause a change in electron affinity and give rise to a depletion region under the surface. The surface sheet resistance is reduced by the depletion region and the barrier heights in diode junctions are more often determined by the surface states than by the electron affinity of the infinite crystal. Surface charge and states are light-dependent and consequently so are device characteristics.

Surface states are dealt with again in relation to diode barrier calculations in section 4.3.

2.2 CSIRO Fabrication Process

In this section a description of the fabrication process of the CSIRO Division of Radiophysics is presented. Where applicable, some alternative schemes and their applications are pointed out.

The achievement of high speed integrated circuits with large complexity and propagation delays of 100 ps is restricted by the classical trade-offs [Eden 1982] of achieving very high gate densities and yet very high process yields and achieving low dynamic switching energies with low power per gate. There are various processing schemes which make compromises to suit a particular application. The planar implanted process was developed to achieve very high density and is suitable for complex digital circuits. A mesa process using a wafer grown with Molecular Beam Epitaxy is better suited to low noise analog applications because it avoids crystal damage due to implantation processes. At the CSIRO a seven mask mesa isolation process is used.

2.2.1 Review of CSIRO Fabrication Process

The foundation for GaAs integrated circuit construction is the semi-insulating substrate which is usually high purity semi-insulating GaAs grown by the liquid-encapsulated Czochralski (LEC) process with <100> orientation [Nuzillat et al. 1982]. To avoid substrate problems (back-gating, leakage, light sensitivity, parasitic effects of interface traps etc. [Gloanec et al. 1980]) a 2 to 5 μm epitaxial buffer layer is grown prior to deposition of the active layer [Nuzillat et al. 1982]. At the CSIRO Division of Radiophysics, a Molecular Beam Epitaxy (MBE) machine is used to grow active layers
on commercial substrate wafers (Fig. 2.2).

**Device Isolation Process**

There are two methods for isolating active devices on the substrate. The entire surface can be coated with an active layer and then either etched to form a mesa isolation or selectively bombarded to form insulating regions. Alternatively, the substrate surface can be selectively implanted to form isolated active regions.

In a self-aligned epitaxial process, isolation is achieved by selective bombardment with protons, oxygen or boron to render the epitaxial material semi-insulating [Nuzillat et al. 1982]. An advantage of this process is that a flat surface remains after the isolation process. The scheme can also be used in a self-aligned process in which the gate is used to mask the channel region while the ohmic regions are implanted to improve their conductance. However, the process starts with a single active layer and this restricts the circuit to consist of only one of either enhancement or depletion mode devices.
Planar fabrication techniques have been developed using ion implantation on semi-insulating GaAs substrate. The individual devices are formed by selected implants to give very uniform MESFET devices with high density suitable for VLSI. Two localized implant steps through a thick dielectric mask are made to form device active regions and ohmic contact regions. If both enhancement mode and depletion mode devices are required an extra implant step is used. The process is less prone to contamination by surface states because the surface is protected by dielectric layers throughout the fabrication [Eden et al. 1978a].

Mesa isolation is achieved by etching through the active layer to form a mesa structure typically 0.3 μm deep. Smooth sloping sides are essential to prevent wiring disconnections and techniques have been developed using tapered photo-resist [Dobratz et al. 1980]. There are disadvantages with the mesa approach including an increased fringe capacitance at the edge of the mesa and wiring problems over the mesa terrain. Also, chip area is needed for mesa side walls. Of greater significance is the requirement of a recessed-gate structure so that source-end epi-layer is thick enough to maintain a low parasitic resistance. Enhancement-mode GaAs MESFET devices require precise thickness control which is difficult without using self limiting thinning techniques [Mizutani et al. 1980].

Better low noise microwave devices are made without implant processes and this requires mesa isolation. For this reason, the mesa technique is used at the CSIRO (Fig. 2.3). The first mask in the process defines the mesa structure which must be deep enough so that the active layer is removed.

Metallization

Ohmic contacts are manufactured by depositing a gold germanium (AuGe) alloy onto the semiconductor surface. The contact is alloyed with heat so that the metal diffuses into the semiconductor producing a gradual metal-to-semiconductor transition without the potential barrier of an abrupt junction. A low temperature (400 °C) process is used to prevent dissociation of arsenic. In the CSIRO process the same metal is used for ohmic pads and wiring which are defined by the second mask (Fig. 2.4). A Ni:AuGe:Ni combination is evaporated as a multilayer metallization and then alloyed by annealing.
The most reliable Schottky contacts use titanium-platinum-gold (Ti-Pt-Au) alloy which can be applied with a photo-resist lifting process. Ti-Pt-Au is also used as wiring between AuGe ohmic pads. Other Schottky alloys such as Cr:Pt:Au or Cr:Pd:Au can also be used for wiring.

In the CSIRO process the third mask defines the Schottky metal (Fig. 2.5). Initially aluminium was used for its convenience but its poor adhesion property means it is used for gate and diodes and not for wiring. The Schottky gate is recessed into the GaAs surface by using a chemical etchant or anodising method to set the transistor pinch-off voltage. The non-uniformity of the recessing restricts the process to depletion mode devices.

The fourth CSIRO process mask is the same as the ohmic (AuGe) mask except that all features are slightly smaller. It is used to lay gold over the ohmic metal to improve the electrical properties and it sandwiches the Schottky metal where that contacts the AuGe ohmic contact metal (Fig. 2.6).
In many processes a second level metal is deposited over a dielectric layer in a manner similar to the first level wiring. However, there is no native oxide for GaAs which complicates the selection of a suitable dielectric and for microwave applications the increased capacitance caused by a dielectric is a disadvantage. Therefore, as is common in other processes, the CSIRO process uses an air-bridge structure.

The fifth mask covers the entire wafer with resist except where the second level metal is to contact the first. Then a thin layer of Gold is deposited over the entire surface. The Sixth mask exposes this gold sheet where the second level metal is required and it is built up by electroplating. The resist and thin sheet of gold are removed by a lift-off process and the result is an air-bridge structure (Figs. 2.7-2.9).

Passivation

The final step in the fabrication process is the deposition of a protective passivation layer with the seventh mask.

Lithography

The limiting factor in the fabrication of high speed circuits is the smallest width of gate line that can be achieved. One micron features can be resolved using reduction photolithography in conjunction with lift-off, plasma etching and ion milling techniques [Long et al. 1982]. However, for sub-micron features it is necessary to use electron beams for direct writing of gates [Mizutani et al. 1980]. At the CSIRO, photolithography masks are used and a direct write electron beam capability has been developed.
**Figure 2.7.** CSIRO process step 5: A thin gold sheet is deposited over photo-resist and contacts the first level wiring as necessary.

**Figure 2.8.** CSIRO process step 6: The second level metal is electroplated onto the thin gold sheet.

**Figure 2.9.** CSIRO process step 7: The photo-resist and thin sheet are removed with a lift-off process to expose the final second level cross-over.
2.2.2 Process Dependent Parameters

Process changes affect the quality of Schottky junctions and ohmic contacts. The Schottky metal chosen is significant and its properties are required to predict Schottky barrier heights and junction ideality. Alloyed ohmic connections vary with the contact geometry so measured parameters from process samples are required to predict contact resistance [Marlow and Das 1982]. Also, the minimum electrode spacing is restricted by the alignment and lithography tolerances. These parameters are dictated by the capabilities of the fabrication process and they are independent of the type of device constructed with the process.

Two parameters which can be chosen by the designer are the doping level of the semiconductor and the pinch-off potential of the FET devices. All characteristics depend in some way on the doping level and it is necessary to choose correct doping for good overall performance. Device pinch-off potential is dependent upon the depth of the channel and the uniformity between devices is another important factor.

The determination and classification of these parameters is covered in section 4.5.

2.3 Devices

This section gives an outline of the various active devices that can be fabricated on a GaAs substrate. The discussion lists the devices, their modes of operation and the properties that they exhibit because they are fabricated in GaAs. Where applicable, modelling techniques for these devices are presented.

The most established devices are passive components, the Schottky barrier Diode, and the Metal Semiconductor FET (MESFET). Recently the High Electron Mobility Transistor (HEMT) has emerged while the Heterojunction Bipolar Transistor (HBT) technology is still in an infant state.

A comparison of these GaAs devices is presented by Eden [1982].

2.3.1 Schottky Barrier Diodes

Doped Gallium Arsenide forms a diode contact with various metals (e.g. Al, Ti, Pt) and alloys. These junctions form excellent diodes and gate junctions suitable for
MESFET devices. Their potential barrier is of moderate height (0.7 V) and their speed is very high\(^\dagger\). A typical high-performance GaAs Schottky diode of 2 \(\mu\text{m}^2\) area has a capacitance of 2 fF and series resistance of 750 \(\Omega\) giving an inverse RC product in excess of 100 GHz [Eden et al. 1978a].

### Diode Operation

The basic equation for current density through the Schottky junction caused by an externally applied potential, \(V\), [Sze 1985] is

\[
J = qN_c \frac{v_R v_D}{v_R + v_D} \exp \left( -\frac{q \phi_b}{kT} \right) \left[ \exp \left( \frac{-qV}{kT} \right) - 1 \right]
\]  

(2-8)

where

- \(V\) is the potential applied to the semiconductor relative to the metal
- \(v_R\) is the velocity at which electrons are emitted from the metal,
- \(v_D\) is the drift velocity of electrons in the semiconductor,
- \(\phi_b\) is the barrier potential, and
- \(N_c\) is the density of states in the conduction band.

The large influence of barrier potential on the current density is clear from its position as an exponential index. In order to predict diode behaviour it is necessary to determine the barrier potential accurately and to consider its dependence on doping level, temperature and surface states. In addition, through the Schottky effect, the barrier height is influenced by an electric field so that its height is slightly reduced at high reverse bias [Sze 1985].

The barrier potential is weakly dependent on doping as depicted in Fukui’s empirical formula [Fukui 1979] for aluminium:

\[
\phi_b = 0.026 \ln(N_D) - 0.245 \quad \text{[V]}
\]  

(2-9)

Surface states can be included by expressing the potential in terms of two parameters, \(c_1\) & \(c_2\), and the metal work function, \(\phi_m\) [Sze 1985]:

\[
\phi_b = c_1 \phi_m + c_2
\]  

(2-10)

If the fermi level is tied to that of the surface states \(c_1 \to 0\). This occurs when there is a high density of surface states which can be filled in preference to transferring charge

\(^\dagger\) High speed is a property of all metal-semiconductor junctions because there is no recombination time for electrons in metals.
to the metal. On the other hand if the barrier is not affected by surface states $c_1 \rightarrow 1$ and (2.10) would become simply the difference in the work functions (i.e. $c_2$ becomes the semiconductor work function). Measured data [Sze 1985] for GaAs gives $c_1 = 0.07 \pm 0.05$, $c_2 = 0.49 \pm 0.24$ [V].

A method for combining these equations and the inclusion of temperature dependence is dealt with in section 4.3 which develops expressions for diode model parameters.

Fig. 2.10 shows the overall electrical characteristic of a typical Schottky diode and the individual characteristics of phenomena involved. Normal mode of operation in regions of reverse bias, near zero bias and forward bias and extreme modes of operation in resistance and breakdown regions are examined in the following discussion.

When a reverse bias is applied to the junction (large $V$ in 2-8), the emission velocity of electrons into the semiconductor, $v_R$, is much less than the drift velocity caused by the electric field in the semiconductor. In this case $v_R$ dominates the current equation to give the reverse leakage current:

$$J_o = qN_c v_R \exp\left(-\frac{q\phi_b}{kT}\right)$$

(2-11)
This reverse current can also be predicted by the Richardson equation for thermionic emission [Jay 1984]:

\[ J_o = A^* T^2 \exp \left( -\frac{q\phi_b}{kT} \right) \]  

(2-12)

The adjusted Richardson constant, \( A^* \), includes electron mass \( (A^* = A^* m^*) \).

Although apparently independent of \( V \), this current is shown in Fig. 2.10 as a sloped line because the barrier height is lowered by the Schottky effect. In a uniform field, \( E \), the potential barrier is lower than the energy band difference by \( \sqrt{\frac{qE}{4\pi \varepsilon}} \) [Sze 1985]^§. Hence as the reverse potential increases the current flow is increased.

If the junction reverse bias is small, the electron velocity is limited by thermal and scattering effects in the semiconductor and \( \nu_D \) dominates the current density equation. This effect is shown in Fig. 2.10 by the thermionic emission and diffusion lines which produce a negative current.

With a near zero external bias the negative current flow into the semiconductor is not only slowed by diffusion effects but is also cancelled by an equal positive flow into the metal.

At forward bias the flow of electrons is predominantly by emission from the semiconductor into the metal. As the bias increases, the barrier height is decreased and the current density is correspondingly larger. This is depicted by the exponential emission into metal line in Fig. 2.10.

**Resistance**

At high forward bias greater than the barrier potential there is no barrier or depletion layer preventing flow from the semiconductor to the metal. The transport is completely dominated by the drift velocity which results in a resistive characteristic.

---

^§ The effective barrier imposed by the work function difference, \( \phi_b \), can be lowered by imposing an electric field to assist electron emission into the semiconductor. This lowering, known as the Schottky effect or image force lowering, can be expressed mathematically by considering the potential energy possessed by the emitted electron. A potential well is formed by the imposed electric field \( E \) repelling the emitted electron from the metal and the positive charge left on the metal surface which attracts it. The potential energy at a distance \( x \) from the metal surface is

\[ PE(x) = \frac{q^2}{16\pi \varepsilon} + qEx \]

The potential barrier, \( \phi_b \), is lowered by this potential energy which has a minimum \( \Delta\phi \) at \( x = x_m \).

If a uniform field is assumed then,

\[ x_m = \frac{q}{\sqrt{16\pi \varepsilon E}} \quad \Delta\phi = \frac{qE}{4\pi \varepsilon} \]

In these equations the permittivity \( \varepsilon \) is that of the material the electron escapes into.
**Junction Breakdown**

At high reverse bias the junction will break down either by tunnelling or avalanche. A critical breakdown field, \( E_b \), is required to give significant tunnelling current. This breakdown field is a property of the semiconductor.

Avalanche breakdown depends on the population of carriers and is therefore a function of band-gap energy and doping. A universal expression for the breakdown potential of abrupt junctions is given by Sze [1985]:

\[
V_b = 60 \left( \frac{E_g}{1.1} \right)^{2/3} \left( \frac{N_d}{10^{22}} \right)^{3/4} \text{[V]} \quad (2-13)
\]

**Capacitance**

The reversed biased capacitance of the junction is a function of the doping level of the semiconductor as described by the standard equation derived using Gauss’ law†:

\[
C = \sqrt{\frac{2eqN_d}{\phi_b(a)}} \frac{1}{\sqrt{1 - \frac{V}{\phi_b(a)}}} \quad (2-14)
\]

This expression assumes that the depletion of charge from the semiconductor by a reverse bias continues to occur as the bias is increased. However, in a real device once the entire semiconductor is depleted, no more charge is moved and the capacitance reduces to zero. Normally, diodes are operated only in the forward bias region or the size of the semiconductor region is large so that this effect is not encountered during normal operation. However, in MESFET gate junctions and diodes deliberately operated in the reverse mode as capacitors, it is important to account for this depletion limit effect.

---

† The depletion depth, \( a \), is found from Gauss’ law \( \int E \cdot d\sigma = \frac{Q}{\varepsilon} \). Assuming electric field is uniform over \( \sigma \) and \( Q = qN_d a \sigma \) gives an external potential offset by the built-in potential \( \phi \):

\[
\phi_a - V = \int_0^a \frac{qN_a}{\varepsilon} da = \frac{qN_a a^2}{2\varepsilon}, \quad \text{so} \quad Q = \frac{2\varepsilon(\phi_a - V)a}{a} \quad \text{and} \quad a = \left( \frac{2\varepsilon(\phi_a - V)}{qN_d} \right)^{1/2}.
\]

Differentiating \( Q \) with respect to \( V \) gives the capacitance expression.
The capacitance reduction effect has been addressed by Takada et al. [1982] and Statz et al. [1987] in FET charge models. The depletion charge in the semiconductor, $Q$, is expressed in terms of a function of potential, $V_{\text{new}}$, rather than just of the applied potential, $V$:

$$Q = C_{\text{jo}} \cdot 2\phi_b \left(1 - \sqrt{1 - V_{\text{new}} / \phi_b}\right) \quad (2-15a)$$

$$V_{\text{new}} = \frac{1}{2} \left(V - V_{\text{to}} + \sqrt{(V - V_{\text{to}})^2 + \delta^2}\right) \quad (2-15b)$$

This function gently limits maximum reverse potential to $V_{\text{to}}$, which is the threshold potential required to deplete the whole semiconductor. Thus the charge does not change if the reverse bias is larger than the depletion threshold potential. The junction capacitance then reduces to zero when the whole semiconductor is depleted:

$$C = \frac{C_{\text{jo}}}{\sqrt{1 - V_{\text{new}} / \phi_b}} \cdot \frac{1}{2} \left\{1 + \frac{V - V_{\text{to}}}{\sqrt{(V - V_{\text{to}})^2 + \delta^2}}\right\} \quad (2-16)$$

**SPICE Model**

The diode model in the circuit simulation program, SPICE, although intended for use with silicon $pn$ diodes, can be used to model GaAs Schottky barrier diodes. A summary of the diode model in SPICE is presented here and the selection of suitable model parameters is dealt with in section 4.3.

To model diode behaviour, a simplified version of the current density equation (2-8)† is used:

$$J = J_0 \left\{\frac{qV}{e^{NkT} - 1}\right\} \quad (2-17)$$

The ideality factor, $N$, included in the exponential term is necessary for modelling silicon $pn$ diodes but it also allows an enhanced fitting of this simple form to the variation from thermionic to diffusion limited transport in Schottky diodes.

---

†

$$J = qN_c v_{\text{R}} v_{\text{D}} \exp\left(-\frac{q\phi_b}{kT}\right) \left\{\exp\left(-\frac{qV}{kT}\right) - 1\right\} \quad (2-8)$$
Using the .MODEL card parameter symbols of SPICE and Fig 2.11, the DC model and its temperature dependence are given by the following equations:

\[
ID = I_S \left[ \frac{qV}{e^{NkT}} - 1 \right] + G_{\text{min}}V' \quad (2-18a)
\]

\[
I_S = I_{S0} \left( \frac{T_{\text{nom}}}{T} \right)^{XTI} e^{\frac{qEG(T-T_{\text{nom}})}{NkT_{\text{nom}}}} \quad (2-18b)
\]

\[
IRB = IBV \left( e^{\frac{q(V' + BV)}{kT}} \right) \quad (2-19)
\]

The voltage across the current source ID is \(V'\). The parameters used are reverse saturation current, \(I_S\), nominal temperature, \(T_{\text{nom}}\), a temperature coefficient, XTI, the junction breakdown potential, \(BV\), and breakdown current, \(IBV\), and the energy gap potential, \(EG\), which is a constant parameter supplied by the SPICE user (not \(E_g\) in (2-20d) below). The minimum conductance allowed by the program, \(G_{\text{min}}\), (used to ensure convergence) has a default value of \(10^{-12}\) siemens.

The model includes junction capacitance, \(C_J\), and diffusion capacitance, \(C_D\). The junction capacitance expression is based on (2-14) with a modification to remove the discontinuity which occurs in the forward bias region. The diffusion capacitance is included to account for electron recombination time in \(pn\) semiconductor junctions. This is not significant in Schottky diodes because electrons are not stored in metals.
The SPICE diode capacitance equations are:

\[
C_J = \begin{cases} 
    C_{J0} \left(1 - \frac{V}{V_J}\right)^{M} & \text{for } V < FCxV_J \\
    \frac{C_{J0} \left[1 + \frac{M}{V_J (1-FC)} (V - FCxV_J)\right]}{(1-FC)^{M}} & \text{for } V > FCxV_J
\end{cases}
\]  

(2-20a)

\[
V_J = V_J \frac{T}{T_{\text{nom}}} - 2 \frac{kT}{q} \ln \left(\frac{n'_i}{n_i}\right)
\]  

(2-20b)

\[
\frac{n'_i}{n_i} = \frac{T}{T_{\text{nom}}} e^{\frac{-E_g}{2T} \left(\frac{T+1108}{T}\right)}
\]  

(2-20c)

\[
E_g = 1.15 - \frac{1.02\times10^{-4} T^2}{T + 1108}
\]  

(2-20d)

\[
C_D = TT \left(\frac{IS}{NkT} e^{\frac{qV}{NkT}} + G_{\min}\right)
\]  

(2-21)

AC temperature dependence is modelled in terms of an empirical equation for \(pn\) junctions in silicon and is not accurate for GaAs applications. The equation is derived from an expression for built-in potential [Sze 1985]. Comparison of (2-20d) for silicon with (2-1)\(\S\) for GaAs illustrates the inaccuracy of this temperature model for GaAs applications.

Noise Model

A thermal noise source in parallel with the resistance \(RS\) has magnitude \(\frac{\Delta f}{4kT} = \frac{4kT}{RS} \Delta f\). Shot and flicker noise are modelled by a source in parallel with the junction with magnitude \(\frac{\Delta f}{2qID^2} = \frac{2qIDAF}{\left(\frac{KF}{f}\right)} \Delta f\) where \(KF\) and \(AF\) are flicker noise parameters.

2.3.2 Metal Semiconductor FET’s (MESFET’s)

The most established active device for GaAs microwave and digital work is the Schottky barrier Metal Semiconductor Field-Effect Transistor (MESFET). This device is usually a planar structure with a doped semiconductor channel region between drain and source ohmic contacts. A thin strip of metal is used as a gate which forms a Schottky junction with the channel. In principle, its operation is identical to that of any FET. The Schottky barrier prevents gate current flow and the gate-source potential, \(V_{gs}\),

\[ \phi_b = kT \ln \left(\frac{e^\frac{V}{kT}}{\pi}\right) \]  

\(\D\)

\[ E_g = 1.519 - \frac{5.405\times10^{-4} T^2}{T+204} \]  

(2-1)
controls drain-source current flow through the channel under it. The pinch-off or gate-source turn-off voltage, $V_{to}$, of the device is set by adjusting the thickness of the channel either by setting implant depth or by etching the epi-layer to the desired depth.

A depletion mode (normally-on) device is obtained when $V_{to}$ is negative so that the channel conducts at zero gate bias. This is the easiest device to fabricate and logic circuits designed with it are robust against pinch-off variations. The built-in potential of the Schottky barrier allows an enhancement mode (normally-off) device to be fabricated by setting $V_{to}$ to zero. Enhancement mode devices offer circuit simplicity but they restrict the logic swing to that of the Schottky barrier height (0.4-0.6 V). Manufacture of enhancement mode logics with a self-aligned implanted process has been routine in digital circuits since 1986 [Cates 1990]. A standard deviation of $V_{to}$ less than 25 mV is necessary and is a difficult goal for GaAs fabrication techniques using gate recess etching [Long et al. 1982] without self-limiting etch techniques [Chang et al. 1988].

Description of Operation

Field-effect transistor operation is usually divided into three modes. In the linear mode, the drain-source current, $I_{ds}$, is proportional to the drain-source voltage, $V_{ds}$. As $V_{ds}$ increases, the device enters the saturated mode where the current ceases to rise. The third mode is a cutoff mode where no current flows because the channel is completely depleted.

As used in the Shichmann-Hodges model [Shichmann and Hodges 1968], Shockley’s expression [Shockley 1952] is generally accepted as the standard description of FET linear mode drain current:

$$I_{ds} = \beta W_{oo} \left[ 3 \left( d^2 - s^2 \right) - 2 \left( d^3 - s^3 \right) \right]$$

(2-22)

where $s = \sqrt{\frac{\phi_s - V_{so}}{W_{so}}}$ and $d = \sqrt{\frac{\phi_s - V_{so} + V_{ds}}{W_{so}}}$ are the extents of channel depletion at the source and drain ends respectively.
The conveniently defined term, \( W_{oo} \), is as the depletion potential required to deplete the whole channel:

\[
W_{oo} = \phi_b - V_{to} = \frac{qN_d a^2}{2\varepsilon}
\]

(2-23)

where \( \phi_b \) is the gate junction built-in potential. The use of a half-power-law for the terms \( s \) and \( d \) is derived by assuming uniform doping profile in the channel.

The transconductance parameter, \( \beta \), can be derived by determining the resistance of the channel in the limit \( V_{ds}=0 \) when \( s=0 \) (i.e. the resistance of the channel without a gate structure). The expected ohm-law resistance is equated with the drain conductance to give \( \beta \):

\[
\frac{q\mu N_d a z}{L} = \frac{d}{dV_{ds}} \beta W_{oo} \left\{ 3d^2 - 2d^3 \right\} \bigg|_{V_{ds}=0} = 3\beta W_{oo}
\]

\[
\therefore \quad \beta = \frac{q\mu N_d a z}{3LW_{oo}}
\]

(2-24)

where the terms \( z, a, \) and \( L \) are the channel’s width, depth and length respectively.

The saturated mode current is set in the Shichmann-Hodges model to the current given by (2-22) when \( d \) is unity. That is:

\[
I_{ds} = \beta W_{oo} s(1 - 3s - s^2)
\]

This assumes that saturation occurs because the drain end of the channel becomes pinched off.

An alternate expression is the general power-law of order \( n \). The drain current in the saturated mode is empirically derived and is justified by its flexibility and good fit to real devices [Richer and Middlebrook 1963]:

\[
I_{ds} = \beta (V_{gs} - V_{to})^n
\]

(2-25)

The exponent, \( n \), gives the degree of freedom required to fit the model to non-uniform doping profile. This expression is intended for predicting small-signal transconductance in the saturated mode and does not describe the linear mode operation.

† The potential to deplete a channel depth \( a \) is found from Gauss’ law in the same way as equation (2-14) was derived:

\[
W_{oo} = \phi_a - V = \int_{0}^{a} \frac{qN_d a}{\varepsilon} da = \frac{qN_d a^2}{2\varepsilon}
\]
In a short channel device such as a microwave MESFET, saturation occurs because the current carriers reach a terminal velocity in high electric fields. The FET model developed by Pucel et al. [1975] accounts for velocity saturation by dividing the channel into two sections; region I closest to the source has carriers accelerating in a field increasing almost linearly towards the drain and region II at the drain end has carriers travelling at constant saturated velocity (Fig 2.12).

At the interface between these regions the gate to active channel potential is defined as $V_p$ and the portion of the channel which is depleted is $p = \sqrt{\frac{V_p - V_{gs} + V_D}{W_0}}$. Region I, where there is no saturation, can be considered as a FET channel of length $L_1$ with a drain potential $V_p$ and current through it is described by Shockley’s equation (2-22)†.

The saturated drain current in region II, $I_m$, is limited by the saturation velocity and the depth of the undepleted channel. The saturated current is

$$I_m = v_m q N_d a z (1-p) \quad (2-26)$$

where $a$ is the channel depth and $v_m$ is the maximum electron velocity.

Equating $I_m$ with $I_{ds}$ as given by (2-22), (2-23), (2-24), and (2-26) gives

$$L_1 = L \left( \frac{d^2 - s^2}{3} - \frac{2}{3} (d^3 - s^3) \right) \xi (1-p) \quad (2-27)$$

where

$$\xi = \frac{E_s}{W_0}. \quad (2-28)$$

† $I_{ds} = \beta W_0^2 \left\{ 3 \left( d^2 - s^2 \right) - 2 \left( d^3 - s^3 \right) \right\} \quad (2-22)$.
Note that if the drain potential is small enough so that saturation does not occur, $L_1$ from (2-27) could equate to larger than the actual channel length. This is avoided if $V_p$ is limited to the actual drain-source potential.

In region II the electric field is determined entirely by free charges on the drain electrode. Solving the Laplace equation and including the voltage drop across region I, $W_{oo}(p^2-s^2)$, gives an equation for the drain-source potential, $V_{ds}$:

$$V_{ds} = W_{oo} \left( p^2 - s^2 \right) + \frac{2a}{\pi L} \sinh \frac{\pi(L-L_o)}{2a}$$  \hspace{1cm} (2-29)

This equation in conjunction with the above expression for $L_1$, (2-27), can be used to solve for $p$. Then $I_{ds}=I_m$ can be found using (2-26) when $V_{ds}$ and $V_{gs}$ are given.

**Capacitance**

The gate forms a diode junction with the channel and the charge storage under it is similar to that of a diode. In the Shichmann-Hodges model, source-gate and drain-gate diodes are added to model the diode behaviour and the effects of charge storage. This is adequate for long channel JFET’s but accounting for charge storage in small devices is complicated by ballistic effects and the reduction of capacitance near channel pinch-off [Takada et al. 1982].

As described in the discussion of diode charge storage (section 2.3.1), there is a reduction of capacitance when the channel is completely depleted. A scheme for including this effect in FET models was proposed by Takada et al. [1982] and Statz et al. [1987]. The effect was also reported and included in a GaAs circuit simulator, GASSIM, by McKinley [1986].

A very detailed analytic model of capacitance in MESFET devices has been reported by Chen and Shur [1985]. This description uses elaborate implicit relationships to explain and accurately predict the effects of terminal velocity and Gunn domain formation on charge storage in the device.

**Other Second-Order Effects**

Additional second-order effects complicate the behaviour of the MESFET. They include channel length modulation, drain feedback and the reduction in drain current due to temperature increases and negative electron mobility in high fields [Hartgring 1982].
Since the expression for the transconductance parameter (2-24)† is inversely proportional to channel length, the drain current increases as the device length is reduced. It is evident from Pucel’s model that the length of the unsaturated region of the FET reduces as the device moves further into saturation so the current through it must also increase. An equilibrium exists between the lengths of the saturated and unsaturated regions which maintains the same current in both. The observed increase in drain current is said to be caused by the channel-length modulation of the unsaturated region.

In short channel devices where high electric fields are present, the drain potential is able to affect the charge in the channel, the substrate and the surface region between the gate and drain. This is caused by field lines which terminate on the charges in the channel or even by the creation of charges in the substrate under the device. As a result of this control, the pinch-off potential required at the gate electrode to cut off the device depends on the drain potential.

The charges which are generated by the drain feedback have a finite recombination time which gives a frequency dependence to the effect. At low frequencies the charges have time to recombine and respond to the drain potential and the feedback effect is not observed. At high frequencies, the charges cannot respond and the feedback effect is observed.

An extensive discussion of rate dependent anomalies including drain feedback is given by Ladbrooke and Blight [1988]. The change in drain-source conductance has been modelled by a simple series resistance and capacitance which increase the drain conductance at high frequencies [Camacho-Peñalosa and Aitchison 1985]. An extension of this model is the addition of a current between the drain and source which is controlled by the potential at the junction of the series resistor and capacitor [Scheinberg et al. 1988].

As described earlier, the velocity of electrons in GaAs reduces in high electric fields because the conduction electrons move into a heavier energy level. The observed drain current therefore reduces as the drain potential increases. Increased temperature with higher power dissipation also causes a reduction in drain current. Drain feedback and channel-length modulation act to increase drain conductance as the gate bias is increased. However, a decrease in drain conductance is observed which must be accounted for by a drain current reduction effect.

\[ \beta = \frac{q\mu N_d a_2}{3LW_{\infty}} \]  

(2-24)
Analytic Models

More detailed insight into the geometric effects and behaviour of MESFET operation can be obtained with analytical models which solve basic electron transport and Laplace equations. An excellent overview of semiconductor device modelling using analytical techniques is given by Snowden [1985].

An example solution to the transport and Laplace equations is shown in Fig. 2.13. The contours show the carrier density and electric potential under the gate of a MESFET with a 0.5 \( \mu \text{m} \) gate, doped with \( 10^{17} \) carriers per cm\(^3\). The mesh spacing used for the finite difference calculation was 250 \( \AA \). The boundary conditions at the gate, source and drain are fixed potential and charge and, except at the source and drain, Neumann conditions are applied to all surfaces [Snowden 1985]. That is, the gradient of potential and carrier density is zero in the direction normal to the surface so that no current flows across the boundary. This type of modelling requires a large computational effort which is undesirable when simulating circuits with many devices.

An analytical model proposed by Shur and Eastman [1978] divides the MESFET device into regions including depleted, undepleted, transition and Gunn domain. The transition region provides a smooth change between depleted and undepleted regions and the variation of electron velocity is considered. The Laplace equation is applied to
each region to determine the electron transport in the device. This provides a detailed model without resorting to a complete two-dimensional finite difference scheme.

There are other analytical models which use similar implicit schemes [e.g. Lehovec and Zuleeg 1970, Wada and Frey 1979, Ali Khatibzadeh and Trew 1988]. These are useful for determining characteristics of a single device but are not satisfactory for circuit simulation involving more than a few devices.

2.3.3 A Review of Existing MESFET Circuit Models


**SPICE JFET Model**

Since its inception, the SPICE simulation program has included the Shichmann-Hodges JFET model, designed to simulate transistors which saturate only through drain-end depletion, with one adaption. Instead of the Shockley current expression, SPICE uses a three mode square-law of gate bias which can be derived by assuming the electric field is constant along the channel [Middlebrook 1963]:

cutoff mode, $V_g \leq 0$

$$I_{ds} = 0 \quad (2-30a)$$

linear mode, $0 < V_g$ and $V_{ds} \leq V_g$

$$I_{ds} = \beta (1+\lambda V_{ds}) \frac{1}{2} V_g \left( V_{ds} - V_{dscl} \right) \quad (2-30b)$$

saturated mode, $0 < V_g$ and $V_{ds} > V_g$

$$I_{ds} = \beta (1+\lambda V_{ds}) V_g^2 \quad (2-30c)$$

where $V_{gs} = V_{gs} - V_{to}$ and $\lambda [V^{-1}]$ is a channel-length modulation parameter.

The gate junction diode behaviour is modelled by two diode elements which are identical to the SPICE diode model except that the ideality factor is internally set to unity. DC temperature dependence of the diode reverse saturation current, $I_s$, is the same as the diode model.
Charge storage is modelled by ideal gate-source and gate-drain diode junction capacitances described by an inverse half-power-law of junction potential, as in (2-14)†, with the same temperature dependence as the diode model.

Thermal noise sources with magnitudes \( \frac{IR_S^2}{RS} = \frac{4kT}{RS} \Delta f \) and \( \frac{IR_D^2}{RD} = \frac{4kT}{RD} \Delta f \) are in parallel with the gate and drain resistances, RS and RD, respectively. Thermal and flicker noise is modelled by a noise source in parallel with the drain current source with magnitude \( IN = 4kr_2g_{na}\Delta f + KF \frac{ID}{f} \Delta f \) where \( g_{na} = \frac{\partial ID}{\partial V_{gs}} \) and KF and AF are flicker noise parameters.

**Curtice Model**

The SPICE JFET model is not adequate for describing saturation due to velocity limiting because the saturation knee in a short channel FET actually occurs at a lower drain potential. The n-channel GaAs MESFET model developed by Curtice [1980] and installed in SPICE by Sussman-Fort et al. [1984] overcomes this with a hyperbolic tangent function which gives an adjustment for the saturation knee potential:

\[
I_{ds} = \beta (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds})
\]  

(2-31)

The saturation parameter, \( \alpha [V^{-1}] \) determines the saturation potential.

\[
C = \sqrt{\frac{\varepsilon qN_t}{2\phi_t}} \frac{1}{\sqrt{1-V/\phi_t}}
\]  

(2-14)
A Discrete Element Subcircuit

The implementation of the Curtice model in early versions of SPICE such as 2g7 requires complex modification to the program code [Sussman-Fort et al. 1984]. To avoid this a lumped element equivalent circuit using the existing devices can be configured to give a similar response.

A subcircuit implementation of the Curtice model [Curtice 1980] shown in Fig. 2.15 was developed as part of this work and reported in a paper reproduced in Appendix section 9.2 [Parker and Skellern 1987]. The square-law behaviour of the JFET held in saturation by a 100 V source is multiplied by a hyperbolic tangent function generated by the current flowing through two back-to-back diodes, DTANH1 and DTANH2. The diode model parameters are set so that the reverse current is $\tanh(\text{Bias Voltage}) \mu \text{A}$ with no frequency or temperature dependence (IS=1 $\mu \text{A}$, N=19.4, EG and XTI=0). The voltage applied to these diodes by ETANH is $\alpha V_{ds}$. The current-controlled-current-source FMESFET is a two-dimensional nonlinear source controlled by the product of the currents through the JFET and the diodes (sensed with the voltage source, VTanh). The parameters BETA, VTO, PB, IS & CGS of the JFET are set to those of the final MESFET. Thus the controlled source's current is as required by (2-31). Discrete diode elements, to simulate the gate junction, and parasitic elements can be added as required. A non-zero LAMBDA can be included by using a three dimensional source for FMESFET.

Another lumped element subcircuit MESFET used by TriQuint Semiconductor Inc. [Rosario 1987] adjusts the saturation knee voltage by using a voltage-controlled-voltage-source. The controlled source reduces the gate-source potential of the MESFET by a factor, $\gamma$, before applying it to a JFET element as shown in Fig 2.16. The net result is a model described by
where the JFET parameters VTO, BETA and LAMBDA are derived from the final MESFET parameters $\frac{V_{ds}}{\gamma}$, $\gamma \beta$ and $\lambda$ respectively. The JFET is used purely as a current source with all other functions disabled by default settings and by making IS small ($10^{-30}$).

**Modified Curtice Models**

The square-law function of gate bias is not accurate for short channels and this is a major disadvantage of the original Curtice model, equation (2-31), especially for predicting small-signal behaviour. Also, the capacitance model does not predict reduction in capacitance when pinch-off occurs [Takada et al. 1982]. Sussman-Fort et al. [1986] replaced the square-law with a general power-law and used the exponent as a fitting parameter. He also included the Takada et al. capacitance model. An additional error is the occurrence of drain-source current saturation at a fixed potential determined by the parameter $\alpha$. This is clearly not the case in real devices and the implementation of McKinley [1986] corrected this by making $\alpha$ a function of gate-source potential. There are still shortcomings with these implementations including an asymmetrical charge storage model and the omission of second-order effects such as drain current reduction and drain feedback.

Curtice and Ettenberg [1985] addressed the shortcomings associated with equation (2-31) by replacing the square-law with a cubic polynomial with four fitting parameters. They also included the effect of drain feedback as a modulation of the gate-source potential by the drain-source potential. This model requires a fitting routine for determining the cubic coefficients.
**SPICE3 MESFET Model**

The Statz et al. [1987] MESFET expression is based on the Curtice [1980] model and is included in version 3 of SPICE:

\[
I_{ds} = \begin{cases} 
\frac{\beta V_g^2}{1+b V_g} \left(1+\lambda V_{ds}\right) \left[1-\left(1-\frac{\alpha}{3} V_{ds}\right)^3\right] & V_{ds} < \frac{3}{\alpha} \\
\frac{\beta V_g^2}{1+b V_g} \left(1+\lambda V_{ds}\right) & V_{ds} > \frac{3}{\alpha}
\end{cases}
\]  

(2-33)

where \( V_g = \phi_b - V_{gs} \).

The cubic function is a close approximation of the hyperbolic tangent function proposed by Curtice and contains the saturation parameter, \( \alpha \). The term \( b [V^{-1}] \) is called a **doping tail extending parameter** and gives the ability to deviate from the square-law.

Two SPICE diode elements are included but unlike the previous models the capacitance is modelled by a single charge under the gate rather than independent charges in each diode. This charge sharing scheme is symmetrical between source and drain and this gives the model an advantage for modelling transient conditions with device reversal and pass transistors in logic circuits. It also includes the reduction in gate-source capacitance at pinch-off.

The total gate charge, \( Q_{gg} \) is given by a symmetrical function of \( V_{gd} = V_{gs} - V_{ds} \) and \( V_{gs} \) :

\[
Q_{gg} = 2C_{gs} \phi_b \left(1-\sqrt{1-\frac{V_{new}}{\phi_b}}\right) + C_{gd} V_{eff2} \]  

(2-34a)

\[
V_{eff1} = \frac{1}{2} \left( V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2} \right) \]  

(2-34b)

\[
V_{eff2} = \frac{1}{2} \left( V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2} \right) \]  

(2-34c)

\[
V_{new} = \frac{1}{2} \left( V_{eff1} - V_{lo} + \sqrt{(V_{eff1} - V_{lo})^2 + 0.2^2} \right) \]  

(2-34d)

The junction capacitance is found by differentiation.

If the source and drain potentials swap, the model reverses over a range determined by \( \Delta \) which is set to \( \frac{1}{a} \) in SPICE. In addition, the capacitance is limited to a constant maximum in the forward bias region in order to prevent a discontinuity at \( V_{new} = \phi_b \).
This format was introduced earlier in this chapter in section 2.3.1 as a suitable capacitance model for the diode; note the similarity between (2-34d) and (2-15b)\(^\dagger\).

The SPICE3 MESFET model provides reasonable accuracy for many applications but can be improved for modelling large signal behaviour. The dc model fails to address the change in saturation potential with gate-source potential and the small-signal model is not accurate over the entire operating region of the device. Although the charge storage model is a marked improvement over the previous schemes, it ignores fringing components and it is not adjustable in the forward bias region. Also, the second-order effects of drain current reduction and drain feedback are not included.

**Other Models**

TriQuint’s Own Model (TOM) [McCamant and Smith 1989] is based on the SPICE3 MESFET model. The effect of drain feedback is added by modulating the pinch-off potential with the drain potential as used by Curtice and Ettenberg [1985].

\[
V_{to} = V_{to} + \eta V_{ds} \tag{2-35}
\]

Also, a reduction in drain conductance is included by a scaling function of drain potential.

\[
I_{ds} = \frac{I_{ds}}{1 + \delta V_{ds}/I_{ds}} \tag{2-36}
\]

Other models have been reported which use computationally intensive calculations and transcendental functions [Hill 1985, Johnson et al. 1987, Larson 1987, Madjar 1988, Scheinberg et al. 1989]. These improve the SPICE model but their complexity is not desirable in a circuit simulator.

**2.3.4 Other Active Devices**

**High Electron Mobility Transistor**

A device which provides even better performance than the MESFET in the 1 to 100 GHz range is the High Electron Mobility Transistor (HEMT or modulation doped FET (MODFET)) [Smith and Swanson 1989]. It takes advantage of the greatly reduced electron scattering by donor impurities possible in lightly doped or pure GaAs. In simple

\[
V_{new} = \frac{1}{2} \left( V - V_{to} + \sqrt{(V - V_{to})^2 + \delta^2} \right) \tag{2-15b}
\]
terms, a MESFET structure is formed with a doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ epi-layer which forms a heterojunction with the GaAs substrate. A quantum well on the undoped GaAs (substrate) side of the junction receives free electrons from the donors in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer and these form a thin sheet of electrons with a very high mobility. A review of HEMT manufacture and operation is given by Hill and Ladbrooke [1986] and a review of operation and digital applications is given by Solomon and Morkoç [1984]. Ring oscillators with 12.2 ps propagation time have been reported [Morkoç and Solomon 1984, Solomon and Morkoç 1984]. Fabrication techniques have been improved to allow production of larger circuits such as 2000 transistor multipliers and adders [Leung et al. 1989] and a 4K gate array [Kajii et al. 1988].

**Heterojunction Bipolar Transistor**

The GaAs Heterojunction Bipolar Transistor (HBT) has an inherent threshold uniformity and a bandwidth from 5 to 10 times that of MESFET's [Eden 1982]. For power amplification the HBT exhibits high thermal resistance but for switched circuits it offers superior power density and speed [Long 1989]. The requirement for a buried collector structure complicates the fabrication process.

**JFET**

JFET's can be fabricated using a $p+$ gate stripe to form the $pn$ diode. The operation is similar to a MESFET with an advantage of increased gate barrier potential ($\approx 1.4$ V) which improves the input logic swing capability of enhancement mode devices. It can be difficult to control the $p+$ depth and hence the pinch-off potential and the speed performance is not as high as MESFET's [Long et al. 1982].

**MOSFET**

Implementation of MOSFET technology would ameliorate the input voltage swing limitation. An enhancement mode MOSFET logic circuit has been demonstrated with 110 ps gate delays and 3 volt logic swing [Yokoyama et al. 1980]. However, this is very difficult because stable oxides are not easily achieved, so the gate threshold changes with respect to prior input signal history. In recent years Metal Insulator Semiconductor FET's (MISFET's) using HEMT structures have been reported [del Alamo et al. 1988 and Hida et al. 1989]. The use of InP for MISFET's may be more promising than that of GaAs [Messick 1980] and high speed enhancement mode InP MISFET's have been developed [Antreasyan et al. 1989].
2.3.5 Passive Components

Passive components: resistors, capacitors and inductors can be readily constructed on the GaAs substrate. Resistors can be formed with NiCr deposition or with gate-less FET structures. Metal-insulator-metal capacitors and spiral inductors formed with air-bridge wiring are possible. These components are included in MMIC devices such as those developed at the CSIRO Division of Radiophysics [Goonan et al. 1987]

2.4 Digital Logic

GaAs digital circuits offer significantly greater speed-power product than Si and have become widely available through commercial foundry services.

2.4.1 Survey of Logic Gate Architecture

Topologies for implementing digital logic vary depending on the type and maturity of the fabrication process. Initially, only depletion mode devices with widely varying characteristics were available and logic designs were tailored to accommodate them. As processes improved and other devices became available, different topologies using enhancement mode devices have become possible. Typical logic gates using the various enhancement and depletion mode topologies are illustrated in Fig. 2.17.

Depletion-Mode Logic

The easiest devices to fabricate are depletion mode MESFET's. Designs using them are robust against process and pinch-off variations because of higher logic swings. The disadvantage is the need for twin supply rails and level shifting networks to give the negative potential required to switch off the devices. Three basic topologies exist and are shown in Fig. 2.17; buffered FET logic, unbuffered or Schottky diode FET logic, and source coupled FET logic. Others are hybrids of these. In essence, both an inverter and a level shifting stage form the basic logic functions.
Buffered FET Logic (BFL)  
Schottky Diode FET Logic (SDFL)  
Capacitor Coupled FET Logic (CCFL)  
Direct Coupled FET Logic (DCFL)  
Source-Coupled FET Logic (SCFL)  
Current Steering Logic

*Figure 2.17. Various GaAs FET logic family topologies.*
In Buffered FET Logic (BFL) the level shifting stage uses a source follower and diode configuration which provides a buffer with high drive capability. The various logic functions are performed in the inverter stage by a combination of single- and dual-gate transistor switches. This topology was first demonstrated by van Tuyl and Liechti [1974] and led to a mature 4 GHz logic family [van Tuyl et al. 1977].

BFL power dissipation is high (refer Table 2.2) although lower threshold devices can be used to reduce power dissipation with little sacrifice in speed. BFL has higher fan-out capability but fan-in is limited by the drain capacitances of the input transistors and device area. A NAND gate with more than two inputs is not possible because the voltage drop in the lower series FET's result in a logic threshold shift at the input of the upper transistor [Long et al. 1982].

Schottky Diode FET Logic (SDFL) was developed at Rockwell [Eden et al. 1978b]. In SDFL the various logic functions are performed in the level shifting stage by a ‘wired-OR’ network of diodes. To optimise their reverse-bias capacitance and series resistance the fabrication of the diodes requires a separate process step which gives a lower carrier concentration and lower sheet resistance than the FET channel. Fan-out is limited to 3 without buffering or using wider channels. However, propagation delay is not affected because each load consists of a switching transistor with its own pull-down element [Long et al. 1982].

Source Coupled FET Logic (SCFL) is based on a differential input circuit which gives an inherent low sensitivity to device and logic level variations. Only a single power supply is required but the circuit area is large and with depletion mode devices the power consumption is high [Podell 1983].

Another topology called Capacitor Coupled FET Logic (CCFL) uses a reverse biased diode as a large capacitor to perform the level shifting function. This eliminates the need for the negative supply rail but it must be continually clocked at high speed and a large area is required for the diode. A variation which was Gigabit Logic’s first commercial family is Capacitor Diode FET Logic (CDFL) where the capacitor is added in parallel with the diode chain in BFL or SDFL topologies to increase their maximum switching speed [Eden 1984, Lee et al. 1986]. British Telecommunications Research Laboratories (BTRL) use 1 μm gate length devices in CDFL to achieve 2 Gbit/s processing for optical links [Smith et al. 1989].
Enhancement-Mode Circuit Designs

Enhancement mode devices offer efficient use of area and power but they have a restricted logic swing because the Schottky barrier input cannot be forward biased without drawing excessive currents. A 0.5 V swing is obtainable but requires tight control of the fabrication of very thin active layers. The gate alignment is critical so that the non-conductive regions are totally under the gate otherwise it cannot be turned on. The stringing of input FET’s in series to give AND functions is impractical because of the small logic swings.

Circuits with combinations of resistor loads, depletion mode transistor loads and diode level shifters have been demonstrated. The simplest of these is Direct-Coupled FET Logic (DCFL). The dc fan-out is good in DCFL but switching speeds are reduced by capacitor loading. There is a compromise between high speed and low power consumption. The use of an active load current source made with a normally-on FET sharpens the transfer characteristics and improves speed-power product and speed. This requires an extra fabrication step to produce the depletion-mode device. Typical supply is 3 V and logic swing is between 0.2 and 2.4 V. The complexity of these circuits is limited by fabrication technology and threshold uniformity [Cates 1990].

A recently prominent application is Source Coupled FET Logic using both depletion and enhancement mode devices to reduce the power consumption to as low as 250 μW/gate. The differential inputs are stacked to form a current steering logic illustrated in Fig. 2.17. One gate can implement complex functions which would otherwise occupy large circuit area in conventional SCFL. GigaBit Logic offers a standard library and ‘application specific’ IC’s up to 15,000 gates in Source Coupled Logic [1989 GigaBit Logic Data Book].

2.4.2 Selection of Logic Architecture

Table 2.2 lists the characteristics of the various logic families. Although BFL is power hungry and requires a large area it has the advantage of being very tolerant of process variations. For this reason it is preferred for developmental work especially with an evolving fabrication process. SDFL consumes less power but it has about half the speed, is less tolerant of process variation and has a lower fan-out capability than BFL. Although SCFL is tolerant of process variation, it is much larger and the current steering format is more difficult to design because the various logic levels of the stacked differential inputs must be within reach of the cell output with the matching level. The other families require a much more mature and stable fabrication process. It is clear
that the best results with the infant CSIRO fabrication process will be achieved with buffered FET logic.

### 2.5 Summary

This chapter has summarized the current state of those aspects of GaAs technology relevant to the development of a digital circuit design system for the CSIRO fabrication process. The four aspects discussed are the fundamental properties of GaAs, the fabrication process, the operation and modelling of active devices and the various implementations of digital logic.

The important electron transport properties of the GaAs crystal are its band-gap energy, electron mobility and saturated electron velocity. These properties have been surveyed and their dependence on doping and temperature given. Surface states are identified as having a significant influence on surface resistance, rectifying junctions and ohmic contacts.

The mesa based fabrication process used by the CSIRO Division of Radiophysics has been described. Currently only Schottky barrier diodes and depletion mode MESFET’s are available although the HEMT is under development. Two parameters which can be chosen by the designer are the doping level of the semiconductor and the pinch-off potential of the FET devices.
The SPICE diode model is easily applied to Schottky diodes but the JFET model is not suitable for MESFET's. A review of MESFET models has been given including a simple lumped element SPICE subcircuit model developed by the author. The review gives an historical progression from detailed analytical models such as a two-dimensional solution to the basic transport equations calculated by the author, through the implicit model of Pucel et al. [1975], to the Statz et al. [1987] MESFET model installed in SPICE. The accuracy of MESFET models for the SPICE simulator is limited by deficiencies in the charge storage and small-signal descriptions and the omission of second-order effects. Models with improved accuracy in these areas have a large overhead in computational effort.

Three basic topologies of depletion mode logic are buffered, unbuffered and source coupled. Of these buffered FET logic (BFL) has the advantage of being very tolerant of process variations and is preferred for developmental work.

The first requirement for the development of logic design technique is a model for understanding and simulating MESFET behaviour. The next chapter presents a MESFET model which is an improvement on those presented so far.
2.5.1 Chapter 2 References


Chapter 2: Background - GaAs, the Process, Device Physics, and Digital Logic


3 New FET and MESFET Models for SPICE

3.1 Introduction

The accuracy of a circuit simulation program depends upon the ability of its models to match the detail of device operation. Simulation experience, continuing advances in technology and new applications inevitably reveal model inaccuracies or deficiencies. These give rise to a continuing need for model refinement or new model development. GaAs MESFET circuits are by no means an exception. In particular, the need for short gate lengths in field-effect transistors has introduced high electric fields and ballistic effects which must be taken into account.

For mixed microwave analog and digital circuits, the SPICE circuit simulator allows device level study, exploration of novel circuits and investigation of the effects of fabrication process imperfections. For GaAs MESFET’s, the SPICE JFET model is inadequate, and, as noted in Chapter 2, alternative simple models [Curtice 1980, McKinley 1985, Sussman-Fort et al. 1986] have evolved into the SPICE version 3 MESFET model developed by Statz et al. [1987]. Experimental work in this thesis has demonstrated shortcomings with the charge storage model and the omission of second order effects needed for accurate large-signal transient simulation. This chapter reports the development of improved FET models for SPICE. A computationally efficient extension to an improved SPICE JFET model is presented. The new model has been successfully used to predict large-signal transient behaviour.
The discussion begins by identifying the limitations of the existing SPICE JFET and MESFET models and the historical context of their development. The requirement for better models leads to a description of an improvement to the JFET model which forms the basis for a new unified JFET/MESFET model. The development of the unified model is presented with the inclusion of second-order effects and charge storage. The new model is demonstrated with experimental data. Finally, second-order effects necessary for use in applications beyond the scope of this thesis are identified.

3.1.1 SPICE

SPICE release 2 is a public domain version written in Fortran and released before the development and rise of interest in short channel MESFET devices. Only the JFET model is included and even for simulation of JFET's the predicted small-signal behaviour is valid only in regions where the square-law matches measured large-signal behaviour. The JFET model is definitely not adequate for MESFET devices. It is necessary to provide a MESFET model for this version of SPICE either with a lumped element subcircuit (as described in section 2.3.3) or with a major modification to the program. There are many approaches to this which have been developed to suit specific applications [Curtice 1980, McKinley 1985, Sussman-Fort et al. 1986, Larson 1987, Statz et al. 1987, Curtice 1985].

SPICE release 3b1 is a rewrite in C and incorporates a UNIX-based interface [Quarles 1989]. The device descriptions are separated into modules which are quite easy to modify. The Statz et al. [1987] MESFET model is included but its accuracy is limited. The best-fit large-signal characteristic yields a small-signal model which is valid only over a small operating region [McCaman Smith 1989]. This arises because of an inability to account for doping profile accurately and the omission of important second-order effects. They include the effect of reduction of drain-source conductance and the modulation of the pinch-off potential by drain potential feedback [Hartgring 1982]. Other models [Curtice 1985, Larson 1987, Scheinberg et al. 1989] improve the large-signal model but use computationally intensive non-integral power functions or hyperbolic and logarithmic functions which prolong simulation and are unattractive for SPICE.

In addition, the charge model requires modification for a better match to real devices. The JFET model does not have symmetrical charge sharing nor does it account for the reduction in gate-source capacitance at pinch-off. The MESFET model includes these but eliminates the forward bias capacitance description found in the JFET model and lacks any residual capacitance in cutoff mode. Both are required to match accurately real devices.
The status of FET models is divided between the MESFET models, which in general assume that the short channel effect of velocity saturation dominates, and the JFET model which ignores velocity saturation. No model is accurate when applied to medium length gates. This is a particular handicap when both medium and very short channel FETs are used in a combined analog and digital application. In order to exploit the power of SPICE as a tool for device level study, devising novel circuits and exploring fabrication process variations, there is a need for a single accurate FET model which accommodates all device lengths, adapts correctly to doping profile and provides the second-order and capacitance effects observed in real devices.

3.1.2 Desired Model Characteristics

In SPICE, it is especially important to have an accurate large-signal description because the small-signal model is derived directly from it by differentiation at the operating point. Also, saturation due to pinch-off and terminal velocity must be considered simultaneously in order to model devices of various channel lengths. Required short channel and second-order effects are channel-length modulation, drain feedback and the reduction in saturated drain conductance as gate bias increases. Another particularly important requirement, especially for GaAs enhancement mode devices, is the ability to cater for variations in doping profile. Finally, an accurate model of charge storage is required.

Technical limitations are imposed by the SPICE algorithm. The models must be a well-behaved continuously differentiable function. The drain conductance at saturation and the transconductance at pinch-off should be zero. A very important consideration for simulator speed is avoidance of transcendental functions.

3.2 Improving the Basic JFET Model

The JFET model in SPICE is a good basis for a general long and short channel FET model. The JFET and, indeed, the level 1 MOSFET dc models in SPICE [Quarles 1989] use a simple square-law relation which often does not closely fit real device transfer characteristics. Better results can be achieved with general power-law relations [Richer and Middlebrook 1963] or the Shockley equation [Shockley 1952] but these are not desirable in software simulators because they are computationally intensive expressions. An expression which is computationally simple and yet provides an accurate fit to measured data has been devised in this project and is presented in Tran. on Computer-
3.2.1 Improved Model

The inability of the square-law to relate properly the small-signal transconductance to drain current is significant. To use the square-law model it is necessary before performing a simulation to select the pinch-off potential and transconductance parameters to suit the purpose of the simulation. A best fit to the large-signal behaviour can correctly predict the operating point but not necessarily the small-signal gain at that point. The model parameters must be adjusted for accurate small signal simulation. Further, the third-order intermodulation product, an important specification for microwave amplifier designs, is not predicted by the square-law characteristic.

Our alternative model is derived from the Shockley expression (2-22)† by using a Taylor expansion to remove the computationally intensive radical functions as shown in Appendix section 9.5.1. The result is a simple extension to the SPICE relation:

cutoff mode, \[ I_{ds} = 0 \]  
linear mode, \[ I_{ds} = \beta(1+\lambda V_{ds}) V_{ds} \left\{ B \left[ 2V_{g} - V_{ds} \right] + A \left[ V_{ds}^{2} + 3V_{g} \left( V_{g} - V_{ds} \right) \right] \right\} \]  
saturation mode, \[ I_{ds} = \beta(1+\lambda V_{ds}) V_{g}^{2} \left\{ B + AV_{g} \right\} \]

where \( V_{g} = V_{gs} - V_{to}, \ A = \frac{1 - B}{W_{oo}}, \) and \( 0 \leq B \leq 1.2 \) is a fitting parameter. The range of \( B \) is restricted to eliminate regions of negative transconductance.

A convenient degree of freedom is provided by the term, \( B \), which is called the ‘doping profile parameter’ because it allows deviation from Shockley’s uniform doping assumption. The expression for saturated drain current very closely follows a general power-law relation of order \( n = (3-B) \) as shown in Fig 3.1 and it does not use a computationally intensive radical function. The power-law match can also be demonstrated by showing that the ratio of the saturated drain current and transconductance are equivalent linear functions of gate bias [Parker and Skellern 1990]. When \( B \) is set to 1, the original SPICE square-law is exactly implemented and when \( B \) is set to 0.60, the model is a very close approximation of the Shockley expression. Typical values of \( B \) range from 0.3 to 0.4 for a doping profile with an extended tail, through 0.6 for a uniform profile, to 0.9 to 1.1 for a negative gradient profile.

\[
I_{ds} = \beta W_{oo}^{2} \left\{ 3(d^{2} - s^{2}) - 2(d^{3} - s^{3}) \right\} \]

†
Figure 3.1. Similarity of the new JFET model to a general power-law. The upper curves are transconductance and the lower are drain current. The general power-law is shown in solid lines and the new model is shown by crosses.

Figure 3.2. The experimental data (\(\times\)), is shown for a GaAs FET with gate length 100 µm and width 200 µm. The new model is shown by solid lines with parameters \(\beta = 330 \, \mu\text{A}\cdot\text{V}^{-2}\), \(V_{t0} = -1.9\, \text{V}\), \(B = 0.66\), \(\lambda = 13\, \text{mV}^{-1}\), and \(\phi_B = 0.7\, \text{V}\). This provides a better fit than the square-law SPICE model, (\(\cdots\,\cdot\)), with parameters \(\beta = 299 \, \mu\text{A}\cdot\text{V}^{-2}\), \(V_{t0} = -1.9\, \text{V}\), and \(\lambda = 13\, \text{mV}^{-1}\).
The essential features of a FET model are present in the new expression. The model is a well-behaved continuously differentiable function. The drain conductance at saturation and the transconductance at pinch-off are zero as expected. Also, the small-signal transconductance and zero bias drain-source conductance are equal so the model still obeys the known result that “the transconductance at zero-gate voltage is equal to the total channel conductance in the absence of the gate structure” [Middlebrook 1963]. When applying the new model to measured data, the pinch-off voltage and doping profile parameters can be graphically determined from a plot of the ratio of drain current to transconductance [Richer and Middlebrook 1963]. The fit of the SPICE square-law model and the new model to measured data from a GaAs FET (Fig 3.2) and an NF510 are compared in the paper which reports this model [Parker and Skellern 1990].

3.3 A New Unified JFET/MESFET Model

The basic assumption used by MESFET models incorporating a hyperbolic tangent function [Curtice 1980, Sussman-Fort et al. 1986] is that the dc drain current saturates at a fixed drain-source potential independent of the gate bias. In reality, a FET which is nearly pinched-off by the gate bias will become fully pinched-off at the drain end before velocity saturation occurs and in this region it is better described by the JFET model. The segregation of the JFET and MESFET models can be eliminated by extending the JFET model so that it considers saturation due to pinch-off and terminal velocity simultaneously.

Saturation due to pinch-off and terminal velocity are considered simultaneously by defining an expression for a critical saturation potential, $V_{sat}$. The linear region is then defined as operating with a drain-source potential less than the saturation potential and is described by the improved form of the existing SPICE JFET model. As in a real device, the linear mode operation is independent of saturation effects and the saturated current is the current reached at the onset of saturation.

3.3.1 The DC Model with Saturation

Detailed descriptions of the saturation effect, such as that developed by Pucel et al. [1975], often involve implicit equations which require iterative calculation. In order to apply such descriptions to a circuit simulator it is desirable to use an equivalent explicit expression. The unified FET model uses a four-mode scheme and is completed in the same manner as the existing SPICE models with source and drain ohmic resis-
tances and diode junctions between the gate and drain and the gate and source. An empirical expression is used to describe the drain-source saturation potential and a smoothly differentiable transition mode between the linear mode and the saturated mode is provided. An approximation to Pucel’s analysis developed in Appendix section 9.5.2 is used to define the drain potential at the onset of saturation, \( V_{\text{sat}} \), as a function of Pucel’s saturation index, \( \xi \), defined in (2-28). The saturation index can be used to indicate the type of saturation. When \( \xi \) is very small, saturation is dominated by velocity limiting. In the other extreme of very large \( \xi \), saturation is due to pinch-off only. The device description is then given by equation (3-2):

cutoff mode, \( V_g \leq 0 \)

\[
I_{\text{ds}} = 0 \tag{3-2a}
\]

linear mode, \( 0 < V_g \) and \( V_{ds} \leq V_{\text{sat}} \)

\[
I_{\text{ds}} = \beta \Gamma (1+\lambda V_{ds}) V_{ds} \left\{ B \left( 2V_g - V_{ds} \right) + A \left[ V_{ds}^2 + 3V_g (V_g - V_{ds}) \right] \right\} \tag{3-2b}
\]

transition mode and saturation mode, \( 0 < V_g \) and \( V_{sat} < V_{ds} \)

\[
I_{\text{ds}} = I_{\text{sat}} + \frac{g_{\text{sat}} V_{sat}^2}{4\xi V_g} \max \left[ 1, 1 - \left( 1 - \frac{\xi V_g V_{ds} - V_{sat}}{V_{sat}} \right)^{\frac{1}{2}} \right] \tag{3-2c}
\]

where \( g_{\text{sat}} = \beta \Gamma (1+\lambda V_{ds}) \left\{ 2B(V_g - V_{sat}) + 3A \left[ V_{sat}^2 + V_g (V_g - 2V_{sat}) \right] \right\} \tag{3-2d} \)

\[
I_{\text{sat}} = \beta \Gamma (1+\lambda V_{ds}) V_{sat} \left\{ B \left( 2V_g - V_{sat} \right) + A \left[ V_{sat}^2 + 3V_g (V_g - V_{sat}) \right] \right\} \tag{3-2e}
\]

\[
V_{sat} = \frac{\xi W_{oo} V_g}{V_g + \xi W_{oo}} \tag{3-3}
\]

The linear mode description is identical to (3-1) with the addition of the term \( \Gamma \) which will be defined in (3-11). The transition is an empirically chosen fourth order polynomial in the region

\[
V_{sat} \leq V_{ds} \leq V_{sat} \left( 1 + \frac{V_{sat}}{\xi V_g} \right) \tag{3-4}
\]

When \( \xi \) is very large, the transition region disappears and the model reverts to the JFET two mode form. This description of the transition mode provides a good empirical match to Pucel’s model as shown in Fig. 3.3.

\[
\xi = \frac{E_{ox} L}{W_{oo}} \tag{2-28}
\]
Small-Signal Behaviour

The scheme used in the unified model is an accurate description of the operation of a real device and, through the doping profile parameter, provides an accurate fit to characteristics calculated from various doping profiles as shown in Fig. 3.4. The transconductance versus dc drain-source current of recess-etched MESFET’s calculated by Anholt and Sigmon [1989] is shown for a Pearson-IV profile†, Gaussian profile and constant-doping (BOX) profile. The new model is a much better fit to this data and the ability of the doping profile parameter, $B$, to adjust for different profiles is clearly shown. Adjusting the doping tail extending parameter, $b$, in the existing SPICE MESFET can match the data only in small regions.

3.3.2 Including Second-order Effects

Second-order effects required for accurate MESFET simulation are channel-length modulation, drain feedback [Hartgring 1982], the modelling of reduction in drain conductance due to local heating and negative electron mobility in high fields.

Channel-Length Modulation

An observed increase in drain current proportional to drain potential is usually attributed to channel-length modulation. Although not supported by simple theoretical description of channel-length modulation (as will be shown in section 4.4.2), the inclusion of a $(1 + \lambda V_{ds})$ factor is necessary to provide a good fit to measured devices

Drain Feedback

Drain feedback or second gate effect is a significant phenomenon in short channel devices [Hartgring 1982] which causes an apparent increase in pinch-off voltage with drain-source voltage. It is caused by electrostatic feedback from the drain which creates extra charge in the channel and allows the drain to act effectively as a second gate. An empirical parameter, $\eta$, can be used to effect the depletion potential modulation as

$$W_{oo'} = W_{oo} + \eta V_{ds}.$$  \hspace{1cm} (3-5)

† The Pearson-IV profile has maximum doping slightly under the surface with a decrease in doping towards the surface and a gradual tail into the substrate.
Figure 3.3. A comparison of the unified model (solid lines) with Pucel’s analysis (×). In this case $L/a = 3$, and $\xi = 0.3$. The curves are for various $V_{gs}$ in steps of 20% of $W_{oo}$. Potentials are normalized with respect to $W_{oo}$.

Figure 3.4. Calculated transconductance of recess-etched MESFET’s versus dc drain-source current for various doping profiles. The new model is shown by solid lines for two doping profile parameter, $B$, values ($\xi = 0.10$) and the existing SPICE MESFET model is shown for various doping tail extending parameter, $b$, values.
An alternative approach is to acknowledge the second gate effect as an increase in the gate potential so that

\[ V_{gs} = V_{gs} + \eta V_{ds}. \] (3-6)

The feedback effect is also influenced by recombination centres or traps in the substrate which can cancel the feedback [Hartgring 1982, Larson 1987, Camacho-Penalosa and Aitchison 1985]. Traps form slowly so the potential resulting from the charge at the recombination centres can be modelled as a delayed drain potential. Mathematically, this can be expressed over transient time steps of \( \Delta t \) as

\[ V_r (t + \Delta t) = V_r (t) + (V_{ds} (t + \Delta t) - V_r (t))(1 - e^{-\Delta t/\tau}) \]

\[ \approx V_{ds} (t + \Delta t) - (V_{ds} (t + \Delta t) - V_r (t)) \left[ \frac{4}{4 + \Delta t/\tau} \right] \] (3-7)

where \( V_r \) is the effective potential of the trap centre and \( \tau \) is the effective recombination time constant.

This formulation is similar to that proposed by Scheinberg et al. [1989] but a polynomial approximation to the exponential term is used to improve simulation speed.

To incorporate pinch-off modulation the effective gate potential dependent upon both a dc feedback parameter, \( \eta \), and ac feedback parameter, \( \zeta \), is defined:

\[ V_g = V_{gs} - V_{to} + \eta V_{ds} + \zeta (V_{ds} - V_r) \] (3-8)

A dc or operating point analysis is performed with \( V_r \) set to zero.

The ac small-signal model is changed to include the effect of increasing source-drain conductance at high frequencies. In the small-signal ac model (3-8) becomes

\[ V_g = V_{gs} + \eta V_{ds} \left( \frac{j\omega}{1 + j\omega \tau} \right). \] (3-9)

so the total source-drain conductance is

\[ G_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{ds}}{\partial V_g} \frac{dV_g}{dV_{ds}} \]

\[ = g_{ds} + (\omega \tau + j) \frac{g_m \eta \omega}{1 + (\omega \tau)^2} \] (3-10)

where \( g_{ds} \) is the dc model conductance term. The added conductance is due to the feedback effect and is a function of the transconductance, \( g_m \), and hence the operating point.
Table 3.1. Parameters of Capacitance Curves Shown in Fig. 3.5. at $V_{ds} = 4$ Volts.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{to}$</td>
<td>VTO</td>
<td>Threshold voltage</td>
<td>-1.15 V</td>
<td>-1 V</td>
<td>-1 V</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>PB</td>
<td>Gate junction potential</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>0.7 V</td>
</tr>
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<td>$F_C$</td>
<td>FC</td>
<td>Coefficient for forward-bias</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>depletion capacitance formula</td>
<td>-0.2</td>
<td>-0.05</td>
<td>0.1</td>
</tr>
<tr>
<td>$X_C$</td>
<td>XC</td>
<td>Capacitance Pinch-off Parameter</td>
<td>0.42</td>
<td>0.37</td>
<td>0.18</td>
</tr>
</tbody>
</table>

Field Dependent Mobility

In short channel FET’s the fields become so high that the field dependence of the carrier mobility should be considered. In GaAs devices, there is a reduction in the electron velocity beyond saturation which is caused by the energy band structure of the compound. To model this effect an empirical scale factor, $\Gamma$, is included:

$$
\Gamma = \begin{cases} 
1 & V_{ds} \leq \xi W_{oo} \\
1 - \frac{\kappa (V_{ds} - \xi W_{oo})^2}{(V_{ds} - \xi W_{oo})^2 + \theta^2 (\xi W_{oo})^2} & V_{ds} > \xi W_{oo} 
\end{cases} \quad (3-11)
$$

There are two parameters which set the shape of the current reduction. The first, $\kappa$, limits the extent of the current reduction and the second, $\theta$, sets the rate of reduction relative to increasing drain potential.

Adjusting $\theta$ and $\kappa$ can also compensate for the reduction in drain current caused by temperature rise as modelled in TriQuint’s TOM (2-36)† [McCamant and Smith 1989].

3.3.3 Charge Storage Model

The Statz et al. [1987] charge storage model provides a good basis for a capacitance model since, unlike the JFET model, it provides correct charge sharing and the effect of capacitance reduction near pinch-off. However, the forward bias capacitance is better described by the original JFET capacitance model. Also, the Statz et al. model does not include the residual capacitance in cutoff mode observed in real devices because charge is being depleted from the region between the source and gate electrodes [Takada et al. 1982].

†

$$
I_{ds} \equiv \frac{I_{ds}}{1+5V_{ds}I_{ds}} \quad (2-36)
$$
A modification to the Statz et al. charge storage model adds the forward bias capacitance description used by the original JFET model and introduces a residue capacitance in cutoff mode. The total gate charge, $Q_{gg}$, is given by a symmetrical function of $V_{gs}$ and $V_{gd} = V_{gs} - V_{ds}$. Junction capacitance is found by differentiating:

$$Q_{gg} = C_{gs} \left( 2\phi_b \left( 1 - \sqrt{1 - F_C} \right) + Ext \right) + C_{gd} V_{eff2}$$  \hspace{1cm} (3-12a)

where

$$Ext = \begin{cases} 
\frac{(V_{new} - F_C \phi_b) + (V_{new}^2 - (F_C \phi_b)^2)}{(1 - F_C)^{3/2}} & V_{new} > F_C \phi_b \\
0 & V_{new} \leq F_C \phi_b
\end{cases}$$  \hspace{1cm} (3-12b)

$$V_{eff1} = \frac{1}{2} \left( V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2} \right)$$  \hspace{1cm} (3-12c)

$$V_{eff2} = \frac{1}{2} \left( V_{gs} + V_{gd} - \sqrt{(V_{gs} - V_{gd})^2 + \Delta^2} \right)$$  \hspace{1cm} (3-12d)

$$V_{new} = \frac{1}{2} \left( (1 + X_C) V_{eff1} - (1 - X_C) V_{to} + \sqrt{((1 - X_C)(V_{eff1} - V_{to})^2 + 0.2^2} \right)$$  \hspace{1cm} (3-12e)

If the source and drain potentials swap, the model reverses over a range determined by $\Delta$ which is set to $V_{sat}/2$ at $V_{gs} = \phi_b$. The term $Ext$ is used in the forward bias region $V_{gs} > F_C \phi_b$ to maintain a straight line relation between gate-source capacitance and gate bias. This is the same scheme used in the JFET model. The parameter $X_C$ is added to set the gate junction capacitance in cutoff mode to $X_C$ times the linear mode value. These additions improve the match of the model to measured data as shown in

Figure 3.5. Experimental gate-source capacitance data from Scheinberg et al. [1989]X, Rosario [1987]•, and Huang et al. [1986] (diamonds). The corresponding modified capacitance model is shown by solid lines. The corresponding SPICE MESFET model is shown by dashed lines. Parameters used are given in Table 3.1.
The parameters used are given in Table 3.1. In the forward bias region the ability to adjust the linear region is a necessity in order to match measurement.

### 3.3.4 Implementation in SPICE

The unified model is installed in the Sydney University copy of SPICE3 as an extension of the existing JFET model. The model is completed with the existing ohmic resistances, RD and RS and diode junctions between the gate and drain and the gate and source. The enhanced list of model parameters is given in Table 3.2. The default parameter values are set to give the standard JFET form. For this reason, the original capacitance model is retained by default and a control parameter is used to select the modified Statz et al. [1987] capacitance model. The use of device and model cards is identical to that for the JFET.

The Statz et al. charge storage transition interval between forward and reverse mode is internally set to half $V_{sat}$ at $V_{gs} = \phi_b$:

$$\Delta = \frac{\xi}{\xi + 1} \left(\frac{\phi_b - V_{in}}{2}\right)$$

### Table 3.2. Model Parameters Specified for New FET Model

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Mnemonic</th>
<th>Parameter</th>
<th>Default Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{to}$</td>
<td>VTO</td>
<td>Threshold voltage</td>
<td>-2.0</td>
<td>V</td>
</tr>
<tr>
<td>$\beta$</td>
<td>BETA</td>
<td>Transconductance parameter</td>
<td>1.0E-4</td>
<td>A/V**2</td>
</tr>
<tr>
<td>$\xi$</td>
<td>XI</td>
<td>Saturation parameter</td>
<td>$\infty$</td>
<td>–</td>
</tr>
<tr>
<td>$\eta$</td>
<td>ETA</td>
<td>Drain feedback parameter</td>
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<td>–</td>
</tr>
<tr>
<td>$\zeta$</td>
<td>ZETA</td>
<td>High Frequency Drain feedback parameter</td>
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<td>–</td>
</tr>
<tr>
<td>$B$</td>
<td>B</td>
<td>Doping profile parameter</td>
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<td>–</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>LAMBDA</td>
<td>Channel-length modulation parameter</td>
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<td>1/V</td>
</tr>
<tr>
<td>$R_{dd}$</td>
<td>RD</td>
<td>Drain ohmic resistance</td>
<td>0</td>
<td>Ohm</td>
</tr>
<tr>
<td>$R_{ss}$</td>
<td>RS</td>
<td>Source ohmic resistance</td>
<td>0</td>
<td>Ohm</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>CGS</td>
<td>Zero-bias gate-source capacitance</td>
<td>0</td>
<td>F</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>CGD</td>
<td>Gate-drain capacitance</td>
<td>0</td>
<td>F</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>PB</td>
<td>Gate junction potential</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>KAPPA</td>
<td>Velocity reduction extent parameter</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>$\theta$</td>
<td>THETA</td>
<td>Velocity reduction rate parameter</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>$\tau$</td>
<td>TAU</td>
<td>Time constant for High Frequency Drain feedback</td>
<td>0</td>
<td>s</td>
</tr>
<tr>
<td>$X_C$</td>
<td>XC</td>
<td>Capacitance Pinch-off Parameter</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td>$F_C$</td>
<td>FC</td>
<td>Coefficient for forward-bias depletion capacitance formula</td>
<td>0.5</td>
<td>–</td>
</tr>
</tbody>
</table>

Fig. 3.5. The parameters used are given in Table 3.1. In the forward bias region the ability to adjust the linear region is a necessity in order to match measurement.
3.3.5 Model Appraisal

The use of the extended JFET model is quite straightforward. As an example, Figs. 3.2 and 3.6 show the characteristics obtained with SPICE for transistors with two gate lengths. The measurements were made by direct probing of devices on wafer (using a Cascade microwave probe set) with dc voltage sources (refer to Appendix section 9.1.5).

The long channel case (Fig. 3.2) shows that the improved JFET model is better able to match the measured data from a long channel device. The short channel case (Fig. 3.6) shows the characteristics of a short channel GaAs MESFET from chip M-1A. In this short channel case the original SPICE MESFET model poorly follows the device characteristics whereas the new model provides an accurate match to the real device. This illustrates that the addition of the second-order effects is essential to match typical microwave MESFETs. It can be argued that the original model can be made to give correct predictions by adjusting parameters for a good fit at the operating point. The pinch-off potential, for example, can be changed to compensate for the drain feedback effect at

![Figure 3.6. Experimental data, ( ), obtained from a GaAs MESFET with gate length 2 \( \mu \)m and width 200 \( \mu \)m is closely approximated by the new model, solid lines, with \( \beta = 12 \text{ mA V}^{-2} \), \( V_{to} = -2.1 \text{ V} \), \( B = 0.6 \), \( \xi = 0.35 \), \( \eta = 0.058 \), \( \lambda = 40 \text{ mV}^{-1} \), \( R_{ss} = 12 \text{ \( \Omega \)} \), \( R_{dd} = 8 \text{ \( \Omega \)} \), \( \kappa = 0.32 \), \( \phi_0 = 0.7 \text{ V} \). The SPICE MESFET model, ( ), uses parameters \( \beta = 11 \text{ mA V}^{-2} \), \( V_{to} = -2.2 \text{ V} \), \( B = 0.35 \), \( \alpha = 2 \text{ V}^{-1} \), \( R_{ss} = 12 \text{ \( \Omega \)} \), \( R_{dd} = 8 \text{ \( \Omega \)} \), \( \lambda = 30 \text{ mV}^{-1} \) and \( \phi_0 = 0.7 \text{ V} \).]
the operating point. However, this requires knowledge of the device operation before the ‘simulation to determine that information’ can be performed. It is far more efficient to use the new model so that variations in operating regions are correctly simulated.

A further example of the use of the unified model is shown in Fig. 3.7. The measured data was extracted from a published graph [Hwang and Itoh 1987].

**Simulation Example**

Consideration of the drain feedback effect can be critical when pushing designs to their limit as is often the case with high speed GaAs circuits. An example of the performance of a digital circuit is shown in Figs. 3.8 and 3.9. The design of a four-input NOR gate was optimised without accounting for pinch-off potential modulation in the model of a typical device. The design was then resimulated after adding pinch-off potential modulation to the model to give a better match to the typical device behaviour. Fig. 3.9 shows deterioration of logic levels and timing response with the more accurate model because the exclusion of pinch-off potential modulation during the design ignores the low level current through the devices in the nominal “off” state.
Figure 3.8. A one micron width model of a MESFET with gate length 1 µm is shown for the new model with parameters $\beta = 280$ mA·V$^{-2}$, $V_{TO} = -1.6$ V, $B = 0.6$, $\xi = 0.15$, $R_{ss} = R_{dd} = 1733$ $\Omega$, and $\phi_B = 0.7$ V. The effect of pinch-off potential modulation, typical of such a FET, is easily modelled with parameters $\eta = 0.080$ and $\lambda = 0.0$ mV$^{-1}$, solid lines. Only an approximate fit is possible without the pinch-off potential modulation, as illustrated with $\eta = 0.0$ and $\lambda = 120$ mV$^{-1}$, broken lines (----).

Figure 3.9. The simulated performance of a 4-input NOR gate is shown using the GaAs FET models in Fig. 3.8. Three inputs are held at the logic LOW while the fourth is switched with a logic HIGH pulse, shown by a thin solid line. The device widths were optimised using the model without pinch-off potential modulation to give the good response shown by the broken line. However, the inclusion of pinch-off potential modulation in the model shows the poorer response, solid line, which would be likely with real devices.
To illustrate the time dependence of the second gate effect the drain current was measured as a function of a sinusoidally varying drain potential for a Mitsubishi MGF-1400 GaAs FET with zero gate bias. The result is shown in Fig. 3.10 along with the simulation curves. This shows clearly that the general trend of increasing conductance and, to a reasonable extent, hysteresis, are correctly modelled. The time constant $\tau$ was set to 0.14 ms as suggested by Camacho-Peñalosa and Aitchison [1985]. The gain of a simple inverter was also measured and simulated with the results shown in Fig. 3.11. The agreement is reasonable for both very low and high frequencies.

Figure 3.10. MGF-1400 MESFET characteristic for various sweep frequencies at $V_{gs}=0$. The simulated curves (solid lines) with $\tau=0.00014$ give reasonable agreement with measured points (o). Parameters used in the simulation are $\beta = 0.0225 \text{ mA V}^{-2}$, $V_{to} = -2.5 \text{ V}$, $\xi = 0.3$, $B = 1$, $\lambda = 0.01 \text{ V}^{-1}$, $\kappa = 0.2$, $\theta = 4$, $\phi = 0.7$, $R_{ss} = 2.9 \Omega$, $R_{dd} = 2.9 \Omega$, and $\eta = 0.012 \text{ V}^{-1}$ which provide a good dc fit to the device characteristics with the enhanced JFET SPICE model.

Figure 3.11. The gain of an inverter vs. frequency. The gain is a function of source-drain conductance. The measured results (o) are predicted reasonably well by the small-signal ac model (solid line). The simulation parameters are the same as for Fig. 3.10.
The transition and hysteresis are not fitted well in the region between low and high frequency. The hysteresis and conductance variations are represented here by a single time constant model. In reality the effect is probably a multiple time constant phenomenon which would need more complicated modelling. However, as noted this simple model provides good agreement both at dc and high frequency. This is adequate (and necessary) for simulating and checking operation of digital circuits at full speed and static states.

3.3.6 Other Effects

The unified JFET/MESFET model satisfies the requirement for accurate simulation of depletion-mode devices used in a mesa isolated fabrication process. For applications beyond the scope of this development, including enhancement-mode devices, it will be necessary to include other second-order effects including subthreshold conduction, gate junction breakdown and mobility reduction in the linear operating region [Eden 1989].

Subthreshold channel conduction is a significant portion of the characteristic of enhancement-mode devices and can be included as a drain-source leakage current. The dependence of this leakage on gate potential must also be considered.

Gate junction breakdown is not included in the JFET model but can be included in the same manner as the SPICE diode model (discussed in section 2.3.1).

The shape of the transition region between linear mode to saturated mode operation is influenced by a gradual reduction of electron mobility with drain-source potential. The omission of this effect in the Pucel et al. model and in the unified JFET/MESFET model is reasonable for depletion-mode technology. However, this transition is significant in low voltage enhancement-depletion mode logic circuits. In this application it will be necessary to make the transition more gradual either by either using a third-order transition region or by introducing a further dependency on drain-source potential.
3.5 Summary

In summary, an improved JFET model suitable for computer simulators has been presented. It uses a simple polynomial extension of the existing SPICE model which allows a very good fit to the standard Shockley expression and also features the flexibility of a general power-law without using a computationally intensive radical function. There is an extra degree of freedom in the form of the ‘doping profile parameter’ which allows the model to match small-signal to large-signal behaviour correctly.

An extension of the new JFET model yields a unified JFET/MESFET model featuring the ability to model a continuous range of device sizes and offering an improved charge storage model. This is achieved by using an accurate linear mode model as part of a four-mode description of drain current. The model takes the unique approach of retaining the JFET description in operating regions where it is applicable. The short channel effects present in MESFET’s are added as applicable.

The advantage of the new model over existing SPICE models is that it can more accurately fit the device characteristics. The new model gives the designer an accurate MESFET model and an improved JFET model which can match small-signal behaviour over an extended operating range.

The extended model has been installed in SPICE 3b1 (and 3c1) in such a manner that by default, the original JFET model is preserved. Its use is straightforward and it has provided accurate simulations without convergence problems.

The inclusion of the MESFET model in SPICE completes the complement of necessary device models for the design of GaAs digital circuits. The next stage is to determine suitable model parameters to use these models and this is the subject of the next chapter.
3.5.1 Chapter 3 References


4 Determination of Device Model Parameters

4.1 Introduction

In this chapter, expressions for SPICE model parameters are derived in terms of the basic electrical properties and the physical details of the devices. Expressions at this fundamental level were necessary for two reasons. Firstly, the number of fabricated devices available for measurement was small so a best fit to average characteristics was not practical. Secondly, the fabrication process was evolving so it was necessary to anticipate the effect of possible changes on device characteristics.

The circuit elements used in GaAs digital applications are characterised in terms of the fundamental material and process dependent parameters. Sections 4.2, 4.3 and 4.4 characterise passive elements, diodes and MESFET’s respectively. The characteristics are determined from equations which can predict their variation across process tolerances. These equations can also be used in a procedure for circuit extraction from physical dimensions and layout geometry. In section 4.5 the fundamental parameters are classified and the variation of circuit element characteristics with these parameters is summarized.
4.2 Passive elements

In real circuits electrical connections have an inherent electrical resistance and conducting components have parasitic capacitance. These reduce the performance of the devices and increase the loading on circuits. It is important to quantify these circuit parasitics accurately and to make allowance for them in the design and simulation phases of circuit development.

4.2.1 Ohmic Contacts

Ohmic contacts are formed by alloying a suitable metal mixture into the semiconductor surface to form a low [but not zero] loss electrical connection to the epi-layer.

Process Dependence

The performance of ohmic contacts is determined by the fabrication process. The metal composition of the alloy, the doping level of the semiconductor and the geometry of the semiconductor between the contact and the device affect the resistance of the contact. The presence of surface states reduces the electrical thickness of the semiconductor and, to complicate the situation further, the epi-layer often has a thin capping layer of heavily doped semiconductor (in order to improve the ohmic contact) which is etched away at the device’s active region. These factors are quite variable and are not easily predicted by purely theoretical methods. Instead, basic measurable properties unique to the process are used to calculate parasitic resistances in each device.

Calculating Contact Resistance

There are three distinct regions in any contact as illustrated in Fig. 4.1:

i. The interface between the metal conductor and the metal-semiconductor alloy with unit area resistance $R_c$.

ii. The metal-semiconductor alloy with sheet resistance $R_a$.

iii. The semiconductor between the contact and the active part of the device with sheet resistance $R_s$. 
In planar contacts the first two regions do not have uniform current density over their total area because the electric field is concentrated at one end. The resistance of a contact with length $d_o$ and width $z$ can be found by using transmission line techniques [Willardson and Beer 1971, Marlow and Das 1982].

\[ R = R_a \frac{L_t}{z} \coth \left( \frac{d_o}{L_t} \right) \]  

(4-1)

where \( L_t = \sqrt{\frac{R_c}{R_a}} \) is defined as the transfer length.

The salient property of the contact is its transfer length because the current flow is predominantly through a strip one transfer length long at the edge of the contact. If the contact is shorter than the transfer length the resistance is dramatically increased. This imposes a practical design limit on the contact’s minimum physical length.

The semiconductor material of length $d_e$ between the ohmic contact and the active part of the device is tapered due to the gate recess etching process. The epi-layer thick-
ness at the contact is reduced by the surface state depletion potential so its effective thickness, \( h_e \), must be determined from the epi-layer sheet resistance. The thickness at the other end is that of the active region, \( a \), which is accurately set by design. The electric fields between the contact and the active region tend to stay in a trapazoidal region under the surface shown in Fig 4.1. Thus the effective electrical depth of this region is the mean of \( h_e \) and \( a \) which increases the sheet resistance by a factor \( \frac{2h_e}{h_e + a} \). The total contact resistance is given by adding (4-1) to give

\[
R = R_a \frac{L_t}{z} \coth \left( \frac{d_o}{L_t} \right) + R_s \frac{d_e}{z} \left( \frac{2h_e}{h_e + a} \right) (4-2)
\]

where \( h_e = (R_s q \mu N_d)^{-1} \).

This equation is useful for extracting the parasitic resistance associated with each ohmic contact and predicting its variation. A circuit extractor can determine resistance from physical dimensions if the process dependent information including material doping level, electron mobility and the three measured resistances are used with the equation. The dependency on process and temperature change is implied in (4-2) because the effective thickness of the epi-layer is a function of mobility and therefore of temperature and doping\(^\dagger\). Also, the physical dimensions are subject to variations caused by the fabrication process.

**Measuring Resistance Properties**

There are several techniques for extracting the three resistance quantities \( R_c \), \( R_a \) and \( R_s \) using a simple geometric pattern of contacts [Marlow and Das 1982]. The simplest arrangement is a collinear set of contacts arranged to provide different separations between adjacent contacts. This technique was selected for test wafers fabricated for this project by the CSIRO. A plot of the resistance between the contacts and their spacing (Fig. 4.2) shows the zero spacing intercept and slope. These correspond to the resistance of both contacts and the epi-layer sheet resistance respectively.

\[\mu = \frac{5.81 \cdot 10^4}{T} N_d^{0.151}\] (2-6)

\(\dagger\)
The end-resistance of three adjacent contacts is given by the ratio of a voltage measured between the centre-contact and one end-contact and a current driven from the centre-contact to the other end-contact. This measurement together with equation (4-1) and a relation between the alloy sheet resistance and the transfer length [Shur 1987] (equation 4-3) can be used to evaluate the alloy sheet resistance and contact resistance:

$$ R_{\text{end}} = \frac{R_a (L/t)}{\sinh(d/L_t)} $$

(4-3)

The example in Fig. 4.2 shows an intercept at 3.68 $\Omega$ (each contact is half this). The measured end-resistance was $R_{\text{end}}=3.8$ m$\Omega$. The evaluated contact resistance, $R_c$, is 2676 $\Omega$.m$^2$, alloy resistance $R_a = 12.7$ $\Omega$.sq and therefore the transfer length is 14.5 $\mu$m. These are typical values for the CSIRO process used at the time.

### 4.2.2 Parasitic Capacitance, Interelectrode and to Ground

Device electrodes and circuit wiring basically consist of thin strips of metal on a dielectric GaAs substrate. As such, there are equivalent lumped capacitance elements between pairs of electrodes and from each electrode to ground.

#### Interelectrode Capacitance

Van Tuyl [1980] has proposed a set of capacitance equations for calculating inter-
electrode capacitance between coplanar metal strips. The equations give the capacitance, $C_C$, between two conductors with length $l$ separated by a distance $d$.

$$C_C \approx \begin{cases} 
1.39 \times 10^{-11} (\varepsilon_r + 1) / \ln\left(4\left(1+d/l\right)\right) & l/d \leq 0.75 \\
2.82 \times 10^{-12} (\varepsilon_r + 1) / \ln\left(4\left(1+2d/l\right)\right) & l/d > 0.75
\end{cases}$$  \hfill (4-4)

This equation assumes that the electrodes are of equal length. This is often not the case especially between a short 1 $\mu$m gate and a 5 $\mu$m drain electrode in a typical MESFET. A better estimate for this case can be obtained by examining the problem from first principles and applying an approximation similar to van Tuyl’s. The exact expression for the capacitance between two unequal coplanar strips in a homogeneous medium is

$$C = 2 \varepsilon \frac{K[\sqrt{1-k^2}]}{K[k]}$$  \hfill (4-5)

where

$$K[x] = \int_0^{\pi/2} \frac{d\theta}{\sqrt{1-x^2 \sin^2 \theta}}$$

is the complete elliptic integral of the first kind [ITT 1979] and the parameter $k$ is a function of the geometry. A detailed derivation of this is given by Smythe [1968]. The term $2 \varepsilon$ becomes $\varepsilon_r (\varepsilon_r + 1)$ when the strips lie in the interface between a dielectric medium and air, as is the case with wires on a GaAs substrate.

The capacitance between two strips with lengths $l_1$ and $l_2$ separated by a distance $d$ is given by setting $k^2 = 1 - \frac{l_1 l_2}{(l_1+d)(l_2+d)}$. Smythe’s derivation for the case $l_1=l_2$ requires $k = \frac{d}{2l_1+d}$ with equation (4-5) returning $2C$. However, the author found that the former expression for $k$ gives the same result with (4-5) returning $C$. Agreement to twelve decimal places was demonstrated by the author with a one thousand interval Simpson’s rule solution to the elliptic integral.

The inverse symmetry between $K[k]$ and $K[\sqrt{1-k^2}]$ can be used to give an approximation to the elliptic integral ratio (4-6) with no more than 5% error as shown in the Fig. 4.3.
Using the approximation gives an improved version of van Tuyl’s method.

\[
\begin{align*}
\frac{K\sqrt{1-k^2}}{K[k^2]} \approx & \begin{cases} 
\frac{1}{\sqrt{2}} \ln \left( \frac{\sqrt{2} k}{\sqrt{2 - k^2}} \right) & k \leq \frac{1}{\sqrt{2}} \\
\frac{\sqrt{2}}{\ln \left( \frac{\sqrt{2} k}{\sqrt{2 - k^2}} \right)} & k > \frac{1}{\sqrt{2}}
\end{cases} 
\end{align*}
\]

(4-6)

Using the approximation gives an improved version of van Tuyl’s method.

\[
\frac{C_z}{z} \approx \begin{cases} 
3.13 \times 10^{-12} (\varepsilon_r + 1) \ln \left( \frac{8.46}{1-k} \right) & k \geq 0.5 \\
2.50 \times 10^{-11} (\varepsilon_r + 1) & k < 0.5
\end{cases}
\]

(4-7)

where \( k = \frac{l_1 l_2}{(l_1 + d)(l_2 + d)} \).

The graph in Fig. 4.4 shows the capacitance between strips with various geometries. Note that the van Tuyl method underestimates interelectrode capacitance between strips of different width. Alternatively, the van Tuyl method can be applied using the dimension of the longer strip, in which case it would overestimate the capacitance.
The general form of the capacitance variation gives rise to a design rule for the minimum spacing between metal wires or pitch of parallel lines. This is limited by the cross talk capacitance between them because the sheet resistance of the intrinsic GaAs substrate between the wires is very high. The coplanar capacitance between metal strips is given in Fig. 4.4 as 0.10 fF/μm when the spacing is equal to the width of the strip. If the spacing is reduced, the capacitance rises dramatically whereas there is little reduction in the capacitance when the spacing is increased. Therefore a good design rule is to limit the minimum spacing of parallel wires to width of the wire. Of course, adjacent power supply lines which carry a dc current are not adversely affected by a capacitance coupling.

**Capacitance to Ground**

The van Tuyl expression for capacitance to ground is

\[
C_{gr} = 2\pi\varepsilon_0 \frac{z \varepsilon^x(w)}{\ln(8h/w)} + \frac{w \varepsilon^x(z)}{\ln(8h/z)} - \frac{\varepsilon_r \varepsilon_a w z}{h} \quad (4-8)
\]

where

\[
\varepsilon^x(x) = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12(h/x)}}
\]

\[w\] and \[z\] are the conductor's width and length and \[h\] is the height above the ground plane. Helix et al. [1982] suggest that this complexity can be avoided by allowing for a...
fixed fringing capacitance to ground of 0.07 fF/µm proportional to the periphery of the metal contact. A better simplification derived by the author is an expression which approximates van Tuyl’s equation (4-8) for all reasonable rectangular geometries.

\[
\frac{C_{gr}}{2(z+w)} = \frac{\pi \varepsilon_0 (\varepsilon_r+1)}{\ln(8h/w)} \text{ (4-9)}
\]

where \( w \) is the contact’s shortest dimension.

The approximation (4-9) is shown in Fig. 4.5 with the capacitance to ground given by van Tuyl’s expression, (4-8). Capacitance to ground from rectangular structures with \( z/w > 1 \) and with \( w > h \) are not well approximated by (4-9). However, such structures have a large short \( (w > h) \) dimension and correspondingly larger long dimension \( (z/w > 1) \). This is not a reasonable geometry because the structure would occupy a large area for no purpose. Rectangular structures \( (z/w > 1) \), either device electrodes or wires, always have a shortest dimension, \( w \), which is small compared with the substrate thickness, \( h \). Square structures \( (z/w = 1) \) can be small electrodes or large bonding pads. Although width-to-length ratios \( (z/w) \) will vary, features of reasonable geometry will always be near the line defined by (4-9).

In summary, fringe capacitance to ground is simply defined as object perimeter multiplied by (4-9) and interelectrode capacitance is given by (4-7). Only the physical dimensions and the material permittivity are required. It is worth noting that for typical design rules the interelectrode and device fringe capacitances do not have a strong

![Figure 4.5. Fringe capacitance per unit length periphery for a metal strip on a GaAs substrate. The approximation (4-9) shown by the thicker line is good for all reasonable rectangular geometries.](image-url)
dependence on electrode spacing. Within an active device they are small compared with the junction capacitance.

As an example, consider a typical 50 μm wide MESFET device on a 200 μm thick substrate with a 1 μm gate separated by 1.5 μm from 10 μm drain and source contacts. The parasitic capacitance elements evaluate to 5.52 fF between gate and drain or source. The original van Tuyl expression (4-4) predicts either 4.3 fF or 5.4 fF depending on which electrode dimension is used (cf = 9 fF gate-drain junction capacitance). The other capacitances are 7.30 fF between drain and source, 9.27 fF from drain and source to ground and 5.42 fF from gate to ground (cf = 80 fF gate-source junction capacitance). Also, a 100 μm square bonding pad has 56.5 fF to ground and a 4 μm × 100 μm wire has 13.6 fF to ground.

4.3 Diode

Diode behaviour and the SPICE diode model have been described in section 2.3.1. The model can be applied by selecting the correct parameters and in some cases adapting them to the existing SPICE equations which are designed for silicon devices. The temperature model, for example, is not appropriate for Schottky GaAs junctions.

4.3.1 SPICE Model Parameters

Physical Dimensions

The planar diode considered here consists of a Schottky metal and ohmic metal strip with width $z$ and lengths $d_d$ and $d_o$ respectively, separated by distance $d_e$ (Fig. 4.6).
Noise Parameters

The development of noise models is beyond the scope of this work. Also, noise analysis is not supported by version 3b1 of SPICE.

Resistance

The diode series resistance is composed of the ohmic contact resistance and the resistance of the epi-layer separating the ohmic and Schottky contacts as described in section 4.2. The thickness of the separating epi-layer is assumed to be the mean of its unetched thickness and the MESFET channel depth because in the CSIRO process the diodes and gates are exposed on the same mask. The SPICE parameter RS sets the model series resistance. Applying equation (4-2) gives:

\[
RS = R_a \frac{L_t}{z} \coth \left( \frac{d_e}{L_t} \right) + R_s \frac{d_e}{2z} \left( 1 + \frac{1}{aR_s q \mu N_d} \right) \tag{4-10}
\]

Built-in Potential

As discussed in Chapter 2, the built-in potential is dependent on the surface states and therefore surface contamination. The barrier height is also dependent on the applied bias due to the Schottky effect and on the doping level which moves the fermi level.

The Fukui [1979] formula for barrier potential (2-9) can be understood by noting that the energy difference between the fermi level and the conduction band is proportional to the logarithm of doping density. Thus (2-9) can be rewritten:

\[
\phi_b = \frac{kT}{q} \ln \left( \frac{N_d}{N_c} \right) - \phi_b(N_d=N_c) \tag{4-11}
\]

A complete expression for barrier potential is obtained by including the effect of surface states with (2-10):

\[
\phi_b = c_1 \phi_m + c_2 + \frac{kT}{q} \ln \left( \frac{N_d}{N_c} \right) \tag{4-12}
\]

This defines the temperature dependence explicitly and implicitly through the variation of \( N_c \) (2-7). The temperature model for variation of junction potential in SPICE considers both these and the variation in \( N_d \) as a function of the band-gap energy

\[
\phi_b = 0.026 \ln(N_d) - 0.245 \quad [V] \tag{2-9}
\]

\[
N_c = N_{col} \left( \frac{T}{300} \right)^{3/2} \tag{2-7}
\]
in silicon (2-20). This is not accurate for GaAs devices but the discrepancy can be ignored because in SPICE the barrier potential is used for the capacitance model in forward bias conditions rather than to describe the reverse saturation current.

The Schottky effect is ignored when setting the SPICE barrier potential parameter, V_J, because it is used only for the capacitance model in forward bias conditions.

**Capacitance**

The usual expression for junction capacitance derived with the Gauss law (2-14) gives the capacitance due to depletion under the Schottky metal. There is also a constant fringe capacitance due to depletion into the ohmic contact region of the device. This fringe depletion can be approximated by a quarter circle cross-section with radius equal to the diode depletion depth [Takada 1982]. The zero bias capacitance consists of both these components:

\[
C_{JO} = d_d z \sqrt{\frac{qN_d}{2\phi_b}} + \frac{\pi}{2} \varepsilon z \quad (4-13)
\]

In general, the grading coefficient, M, depends on the doping profile under the diode and unless measured data is available it can be left at its default value of 0.5. However, if a uniform doping profile is assumed the grading coefficient can be adjusted to maintain the constant fringing capacitance in reverse bias. That is, \( M \) is chosen to satisfy

\[
\frac{C_{JO}}{(1-V/f_b)^M} \approx \sqrt{\frac{qN_d}{2\phi_b}} \frac{1}{\sqrt{1 - V/f_b}} + \frac{\pi}{2} \varepsilon z
\]

Setting \( 1 - V/f_b = e \) produces a good approximation and gives

\[
V_J = V_J \frac{T}{T_{nom}} - 2 \frac{kT}{q} \ln \left( \frac{n_i}{n_i} \right) \quad (2-20b)
\]

\[
\frac{n_i}{n_i} = \frac{T}{T_{nom}} e^{-q \varepsilon \left( E_g - 1.15 \right) \frac{T}{T_{nom}}} \quad (2-20c)
\]

\[
E_g = 1.15 - \left( 0.012 \times 10^{-4} \frac{T^2}{T + 1108} \right) \quad (2-20d)
\]

\[
C = \sqrt{\frac{qN_d}{2\phi_b}} \frac{1}{\sqrt{1 - V/f_b}} \quad (2-14)
\]
The SPICE capacitance coefficient, FC, should also be left at its default value of 0.5 unless a fit to measured data can be used.

High forward bias electric fields cause minority carrier (hole) injection with a minority carrier storage time, $\tau_s$, typically less than $10^{-15}$ s in GaAs Schottky junctions [Sze 1985]. This is negligibly small so that the SPICE parameter TT can be left at the default zero value.

The physical capacitance between the Schottky and ohmic metals is calculated using (4-7) with the geometric parameter, $k$, set using the diode dimensions:

$$k = \frac{d_s d_o}{(d_s + d_d)(d_e + d_d)}$$

(4-15)

This capacitance should be placed in parallel with the diode model in the SPICE circuit description or netlist.

**Junction Breakdown**

A simple analysis of tunnelling breakdown performed by Golio [1988] assumes that the electric field is the ratio of the applied potential and the depletion depth. Then:

$$E_b = \sqrt{qN_d(\phi_b + V_b)}$$

.$$V_b = \frac{2\varepsilon E_b^2}{qN_d} - \phi_b$$

(4-16)

Abrupt junction avalanche breakdown potential is given by (2-13). The breakdown voltage, $V_B$, is the minimum of the avalanche and tunnelling potentials.

$$V_b = \min \left\{ 60 \left( \frac{E_s}{1.1} \right)^{3/2}, \frac{10^{22}}{N_d}, \frac{2\varepsilon E_b^2}{qN_d} - \phi_b \right\}$$

(4-17)

$$C_c = \begin{cases} 
3.13 \times 10^{-12} (\varepsilon_r + 1) \ln \left( \frac{8.46}{1 - k} \right) & k \geq 0.5 \\
2.50 \times 10^{-11} (\varepsilon_r + 1) \ln \left( \frac{8.46}{k} \right) & k < 0.5 
\end{cases}$$

(4-7)
Reverse Saturation Current

Assuming a Maxwellian velocity distribution and a barrier height many times \( q/kT \) above the fermi level, the current density of electrons moving from the metal to the semiconductor is given by the Richardson-Dushmann equation [Jay 1984]. In addition the Schottky effect reduces the barrier potential by \( \sqrt{\frac{qE}{4\pi e}} \) in a uniform field \( E \) [Sze 1985]. The reverse saturation current modified for this effect is given by:

\[
IS = A^* T^2 \exp\left( \frac{-q\left(\phi_b - \sqrt{\frac{qE}{4\pi e}}\right)}{kT} \right)
\]  \hspace{1cm} (4-18)

The adjusted Richardson constant, \( A^* \), includes the effective electron mass in the metal so that \( A^* = A \frac{m^*}{m} \). A reasonable field to use for Schottky effect lowering is the breakdown field for GaAs, \( E_b \).

Doping and temperature dependence is built into the Richardson equation. The SPICE diode model energy gap parameter, \( EG \), and the saturation-current temperature exponent, \( XTI \), used for the temperature modelling of the reverse saturation current (2-18b) should be set to \( N \left[ \phi_b - \sqrt{\frac{qE}{4\pi e}} \right] \) and \( 2N \) respectively to match (4-18).

4.3.2 Emission Coefficient or Ideality Factor

In the forward bias mode, the transport of electrons is determined by thermionic emission and the drift velocity. Both of these effects vary and as the bias changes the importance of each changes. The total current description is therefore quite complex and not purely exponential. At a neutral bias the potential gradient in the semiconductor is zero and the drift mechanism is not present. Electrons are only thermally emitted into the metal with a current density equivalent to \( A^* T^2 \frac{N_d}{N_c} \) which is the Richardson-Dushmann equation (4-18) at zero potential \( (V=\phi_b) \) applied to the number of filled conduction states. The adjusted Richardson constant \( A^* \) includes the electron mass in the semiconductor. The SPICE emission coefficient, \( N \), can be evaluated so that the diode model passes through this point with \( IS \) set by (4-18):

\[
N = \frac{q\phi_b}{kT} \ln \left[ \frac{m^*/m}{m_{sc}/m} \frac{N_d}{N_c} \exp\left( \frac{-q\left(\phi_b - \sqrt{\frac{qE}{4\pi e}}\right)}{kT} \right) + 1 \right]^{-1}
\]

(4-19)

This variation of \( N \) is shown in Fig 4.7.

\[ I_S = IS \left( \frac{T}{T_{nom}} \right)^{XTI} e^{-\frac{qEG(T-T_{nom})}{kT_{nom}}} \] \hspace{1cm} (2-18b)
Equation (4-19) is a departure from the accepted theory that the emission coefficient should be unity.

For a reverse junction the electron flow is from the metal to the semiconductor. The accepted theory determines this current with the Richardson equation which is derived by considering the population of electrons with sufficient energy to mount the barrier by assuming a Maxwellian velocity distribution. The number of electrons with sufficient energy is a function of their effective mass and is found using fermi-dirac statistics.

An error appears to be the use of the mass of electrons in the semiconductor rather than the metal for determining IS. The barrier is inside the semiconductor and it is assumed that the electron population is a function of their mass in the semiconductor. However, the distance between the metal and the barrier is less than a mean free path (otherwise drift velocity due to interaction should be considered) and electrons emerging from the metal will not be affected by the semiconductor before reaching the barrier. The population of electrons with sufficient energy to mount the barrier should be counted in the metal. Therefore, their mass in the metal should be used in the Richardson constant.

Figure 4.7. Variation of diode ideality factor with temperature and doping level.
4.3.3 Twin Diode Model for Planar Effects

In planar devices, a significant resistive component arises with forward bias because the current through the Schottky junction is concentrated at the edge closest to the ohmic contact rather than being spread evenly over the contact.

A transmission line model (shown in Fig. 4.8) can be used to determine the effect of edge conduction on diode current. Consider an infinitesimal diode element of length \( dx \) contributing a current \( di \). If the voltage of the anode (Schottky metal) of this diode is \( V \) the voltage at the cathode is

\[
v(x) = V - \frac{NkT}{q} \ln \left( \frac{di(x)}{dx} \frac{1}{i_s z} \right) \tag{4-20}
\]

where \( i_s \) is the per unit area reverse saturation current of the diode.

The incremental change in cathode voltage is proportional to the epi-layer resistance under the diode metal:

\[
dv(x) = \frac{r_s}{z} dx \ i(x) \tag{4-21}
\]

The solution to this system of differential equations has the form \( i(x) = \frac{A}{xB + 1} \).

Substituting the differential of this equation into the expression for \( v(x) \) with the boundary condition \( v(0)=0 \) gives for an infinite length diode

\[
i = \frac{\sqrt{\frac{2NkT}{q} \sqrt{2qr_s} \sqrt{i_s z \exp \left( \frac{qV}{NkT} \right)}}}{x \sqrt{\frac{qr_s}{2NkT} \sqrt{i_s z \exp \left( \frac{qV}{NkT} \right)}} + 1} \tag{4-22}
\]

*Figure 4.8. Transmission line model of planar diode.*
For a diode with length $d_d$

$$I = \int_0^{d_d} i(x)dx$$

$$= \frac{I_s \exp\left(\frac{qV}{NkT}\right)}{1 + \sqrt{\frac{I_s}{I_d} \exp\left(\frac{qV}{NkT}\right)}}$$

(4-23)

where $I_s = i_s d_d$ and $I_d = \frac{2NkTz}{qr_s d_d}$

Rearranging this equation gives the total voltage drop for the diode:

$$V = \frac{NkT}{q} \ln\left(\frac{I}{I_s}\right) + \frac{NkT}{q} \ln\left(\frac{I}{I_d} + \sqrt{\frac{I}{I_d}}\right) + 1$$

$$\approx \frac{NkT}{q} \ln\left(\frac{I}{I_s}\right) + \frac{NkT}{q} \ln\left(\frac{I}{I_d} + 1\right)$$

when $I_d > I$  (4-24)

**Planar Construction and Effective Diode Length**

It is clear from equation (4-24) that a suitable model of the planar diode is, in fact, two SPICE diode elements in series. The second logarithm is significant when $I$ is near or greater than $I_d$. That is, the effect is significant when

$$d_d \geq \frac{2NkTz}{Iqr_s}$$

(4-25)

This sets a practical limit on the maximum length of the diode necessary to avoid the phenomenon. Also, the same analysis can be applied to the resistance of the Schottky metal line which is fed from one end (eg. from the side of a gate line). In this case $v(x)$ is the voltage along the metal and $r_s$ becomes the sheet resistance of the metal, $r_m$. The resistance of the Schottky metal is significant when

$$z \geq \frac{2NkTd_d}{Iqr_m}$$

(4-26)

If this condition is used as a design rule of maximum diode length then the devices will not exhibit planar effects.

**Example**

Measurements made on MESFET gate junctions have shown that this end effect is present. One example is the current voltage characteristic of the gate junction of the
200 \mu m \times 1.5 \mu m gate on chip M-2(3)L shown in Fig. 4.9. The best fit of a single diode to the low current region requires a large series resistance to fit the high current region. This produces a reasonable overall fit to the data but when the drop due to the assumed resistance is removed from the raw data an absurd non-logarithmic behaviour is observed. The fit to the measured characteristic is improved with a reasonable series resistance and a second series diode with $I_d = 0.822$ mA. The calculated value of $I_d$ for the 1.5 \mu m gate length is 19.1 mA. Therefore, the planar effect is caused by the long 200 \mu m width of the device for which $I_d = 0.8$ mA is reasonable.

Note that the product $NT$ is used as a parameter because it was not possible to measure the junction temperature. This raises the question of whether the large resistance effect can be explained by an increase in temperature at high currents. This is equivalent to an increase in ideality factor when assuming constant temperature. However, a two-fold increase from 300 to 600 K is necessary to fit the data and this is clearly not possible without destroying the device. Therefore, the effect is due to the planar structure. The junction heating does have an influence but is minor and appears as the slight flattening of the 'measured less 15.4 $\Omega$' line in Fig. 4.9.
4.3.4 Diode Summary

With suitable choice of parameters, the SPICE diode model provides a good representation of a Schottky junction and it is possible to select the model parameters from the physical dimensions and properties of the device. The following list gives the parameter extraction equations:

1. IS  Richardson equation for the metal, (4-18)
2. RS  Parasitic resistance, (4-10)
3. N   Ideality factor, (4-19)
4. TT  Default at zero, not significant in Schottky barriers
5. CJO Junction and fringe components, (4-13)
6. VJ  Barrier potential, (4-12)
7. M   default at 0.5 or (4-14)
8. EG  \( N \times V_J \) less Schottky effect reduction, \( N\left(\frac{\phi_H - \sqrt{\frac{qE}{lx}}}{kT}\right) \)
9. XTI 2N
10. KF  Default at zero, noise not considered
11. AF  Default at one, noise not considered
12. FC  Default at 0.5
13. BV  Avalanche or tunnelling, (4-17)
14. IBV Default at 1 mA or set to velocity limited current

If planar effects are significant the resistance parameter should be increased or a second diode element added in series as described by (4-24).

4.4 MESFET Models

MESFET behaviour and the various SPICE modelling techniques have been described in Chapters 2 and 3. These models can be applied by selecting the correct parameters with the aid of the Pucel et al. [1975] model.

The maximum current at the onset of saturation is a function of the maximum electron velocity and the depletion depth of the channel at saturation. The maximum electron velocity is determined from an empirical description for electron velocity, (2-3),
Maximum electron velocity is given by simplifying (2-3):

\[ v_m = v_s \left[ 1 + \frac{E_{m\mu/v_s} - 1}{1 + 0.6e^{(2-10\mu)} + 0.01(E_{m\mu/v_s})^4} \right] \]  

(4-27)

where the maximum velocity field, \( E_m \), is given by an accurate empirical description derived by the author:

\[ E_m = \frac{v_s}{\mu} \left[ 1.015 + 0.39(0.6e^{(2-10\mu)} + 0.01)^{-1/3} \right]. \]  

(4-28)

The depletion depth is determined by considering the drain potential at the velocity saturation potential given by (3-3)\(^\S\) to give, at \( V_{gs} = \phi_b (V_g = W_{oo}) \)

\[ p = \sqrt{\frac{\xi}{\xi + 1}}. \]  

(4-29)

Equation (2-27)\(^\S\) uses the ratio of the low field Shockley expression, proportional to \( \mu \), and the saturated velocity, proportional to \( v_m \). Therefore, the saturation parameter, \( \xi \), is set in terms of \( v_m \) and \( \mu \) so that it will be consistent with its definition in (2-27).

\[ \xi = \frac{E_s L}{W_{oo}} = \frac{v_m L}{\mu W_{oo}} \]  

(4-30)

The saturated portion of the channel continues to increase with increasing drain-source potential as described by Pucel et al. [1975] (2-29)\(^\Y\). The length of the saturated portion, \( L - L_1 \), increases rapidly with drain-source potential until it reaches \( L_{sat} \) when \( \frac{V_{ds}}{W_{oo}} = (p^{2- s^2}) = \frac{\xi}{\xi + 1} \). When the drain-source potential is greater than this empirical condition the change in saturated region length is not so rapid and is considered to be channel-length modulation.

\[ \xi = \frac{E_s L}{W_{oo}} = \frac{v_m L}{\mu W_{oo}} \]  

(2-4)

\[ v_s = 10^5 (0.6 + 0.6\mu - 0.2\mu^2) \]  

(2-5)

\[ E_s = v_s \mu \]  

(2-4)

\[ t = 4 \left[ 1 + 320/sinh(40\mu) \right] \]  

(2-3c)

\[ A = 0.6e^{(10\mu - 0.2)} + e^{-(35\mu - 0.2)} \]  

(2-3b)

\[ \nu(E) = v_s \left[ 1 + \frac{E/E_{c\mu}}{1 + A(E/E_{c\mu})} \right] \]  

(2-3a)

\[ V_{sat} = \frac{\xi W_{oo} V_g}{V_g + \xi W_{oo}} \]  

(3-3)

\[ L_1 = L \left( \frac{d^2 - s^2 - \frac{2}{3}(d^3 - s^3)}{\xi(1-p)} \right) \]  

(2-27)
Maximum MESFET Current

The maximum current is limited by the transistor’s saturation current and is given by (2-26)† when $V_{gs} = \phi_b$ at the onset of saturation. As the device is further saturated this is scaled by the change in length of the unsaturated portion of the channel:

$$I_{\text{max}} = v_m q N_d a z (1-p) \frac{L}{L - L_{\text{sat}}} \quad (4-32)$$

Substituting (4-30) and (4-29) gives a useful design rule:

$$I_{\text{max}} = \xi \frac{\mu W_0}{L} q N_d a z \left(1 - \sqrt{1 + \frac{\xi}{x+1}} \right) \cdot 1$$

$$< \frac{\mu W_0 a z}{L} q N_d \frac{\xi}{x+1} \quad (4-33)$$

This provides an upper limit of MESFET current in terms of known model and material parameters. This limit can be used as the basis for determining maximum power supply current for setting supply rail dimensions.

4.4.1 Existing MESFET Models

Curtice Model

The Curtice MESFET parameters (refer section 2.3.3) can be selected so that the zero bias saturation current and the drain resistance at zero drain voltage are the same as predicted by the Pucel et al. [1975] model. The transconductance parameter, $\beta$, is set to match the saturated current (4-32):

$$\beta (\phi_b - V_{t0})^2 = v_m q N_d a z (1-p) \frac{L}{L - L_{\text{sat}}} \quad (4-34)$$
The terms $v_m$, $p$, and $L_{\text{sat}}$ are given by equations (4-27) to (4-31).

The saturation parameter, $\alpha$, is chosen to match the drain-source conductance, $\frac{\partial I_{ds}}{\partial V_{ds}}$, at $V_{gs} = \phi_b$ and $V_{ds} = 0$:

$$\alpha \beta (\phi_b - V_{to})^2 = q \mu N_d \frac{\alpha \varepsilon}{L}$$ (4-35)

The channel-length modulation parameter, $\lambda$, is described in the later section (4.4.2) on the unified MESFET model. Note that, in these simple models, $\lambda$ should also include the effect of drain feedback.

The MESFET capacitance is modelled by diode junctions which have parameters set to model the gate-source Schottky barrier as already described in section 4.3.1.

**TriQuint Model**

The TriQuint subcircuit model has JFET parameters VTO, BETA and LAMBDA set from the final MESFET parameters as $V_{to}$, $\gamma$, $2\beta$ and $\lambda$ respectively. As in the Curtice model, the transconductance parameter, $\beta$, is set to match the saturated current. The scaling parameter, $\gamma$, is set to $\frac{1}{2} \alpha (\phi_b - V_{to})$ to match the drain-source conductance.

**Statz Model**

The Statz et al. [1987] model provides an extra parameter so that the transconductance can be better matched.

The transconductance parameter, $\beta$, is set so that in the long channel limit ($b=0$), the transconductance $\frac{\partial I_{ds}}{\partial V_{gs}}$ at $V_{gs} = \phi_b$ and $V_{ds} = 0$ is equal to the ohmic resistance of the channel.

$$2\beta (\phi_b - V_{to}) = q \mu N_d \frac{\alpha \varepsilon}{L}$$ (4-36)

The doping tail extending parameter, $b$, is set to match the saturation current:

$$\frac{\beta (\phi_b - V_{to})^2}{1 + b (\phi_b - V_{to})} = v_m q N_d a z \frac{(1-p) L}{L - L_{\text{sat}}}$$ (4-37)

As with the Curtice model, the saturation parameter, $\alpha$, is chosen to match the drain-source conductance at $V_{gs} = \phi_b$ and $V_{ds} = 0$:

$$\frac{\alpha \beta (\phi_b - V_{to})^2}{1 + b (\phi_b - V_{to})} = q \mu N_d \frac{\alpha \varepsilon}{L}$$ (4-38)
The capacitance parameters are described in the next section (4.4.2) on the unified MESFET model.

**Example**

A comparison of these models is shown in Fig. 4.10. The three models have parameters set to match known boundary conditions given by equations (4-34) to (4-38). The device properties and evaluated model parameters are listed in Table 4.1. Fig. 4.10 also shows a measured device with the same physical properties given in Table 4.1. Note that the models do not follow the variation of the measured characteristic with gate-source potential. A better match is obtained with the unified model described in the next section.

### 4.4.2 Unified JFET/MESFET Model

The basic parameters for the unified MESFET/JFET model described in Chapter 3 are determined with the aid of the Pucel model. Parameters for second-order effects such as channel-length modulation and drain-feedback are determined with other models as described below.

**Transconductance Parameter**

At low drain-source potential and near pinch-off, the unified model characteristic is the same as a long channel JFET. Therefore the transconductance parameter is that given by (2-24) for the Shockley expression:

\[
\beta = \frac{q\mu N_d a z}{3 LW_{\infty}} \quad (4-39)
\]

**Channel-Length Modulation Parameter**

The saturated portion of the channel is described by Pucel et al. [1975] in (2-29)† and the length of the saturated portion, \(\Delta L\), is found by inverting this equation and setting \((p^2 - s^2) = V_{sat}\).

\[
\Delta L = \frac{2a}{\pi} \ln \left( \frac{\pi(V_{ds} - V_{sat})L}{2\xi a W_{\infty}} + \sqrt{\left( \frac{\pi(V_{ds} - V_{sat})L}{2\xi a W_{\infty}} \right)^2 + 1} \right) \quad (4-40)
\]

†

\[
V_{ds} = W_{\infty} \left( p^2 - s^2 \right) + \xi \frac{2a}{\pi L} \sinh \left( \frac{\pi(L - L_1)}{2a} \right) \quad (2-29)
\]
Figure 4.10. Comparison of Curtice (Light broken line), TriQuint (Thick broken line) and Statz et al. (solid line) models. The model parameters are listed in Table 4.1. Measured data from a device with the same physical parameters is also shown (circles).

Table 4.1. Model Parameters for a Typical MESFET. The parameters have been chosen to match the nominal dimensions of the MESFET with 200 µm × 1.5 µm gate on chip M-2(3)H.

<table>
<thead>
<tr>
<th>Device Dimensions</th>
<th>( L )</th>
<th>1.5 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>( L )</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>Gate width</td>
<td>( z )</td>
<td>200 µm</td>
</tr>
<tr>
<td>Doping</td>
<td>( N_d )</td>
<td>2×10^{17} \text{ cm}^{-3}</td>
</tr>
<tr>
<td>Pinch-off potential</td>
<td>( V_{lo} )</td>
<td>–3.75 V</td>
</tr>
<tr>
<td>Barrier Potential</td>
<td>( \phi_b )</td>
<td>0.70 V</td>
</tr>
<tr>
<td>Source resistance</td>
<td>( R_{ss} )</td>
<td>7 Ω</td>
</tr>
<tr>
<td>Drain resistance</td>
<td>( R_{dd} )</td>
<td>7 Ω</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Evaluated Properties</th>
<th>( \mu )</th>
<th>4719 cm²/Vs (2-6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility</td>
<td>( v_s )</td>
<td>8.386×10⁶ cm/s (2-5)</td>
</tr>
<tr>
<td>Saturated velocity</td>
<td>( E_m )</td>
<td>3682 V/cm (4-28)</td>
</tr>
<tr>
<td>Maximum velocity field</td>
<td>( v_m )</td>
<td>1.308×10⁷ cm/s (4-27)</td>
</tr>
<tr>
<td>Channel depth</td>
<td>( a )</td>
<td>0.1799 µm (2-23)</td>
</tr>
<tr>
<td>Saturation Parameter</td>
<td>( \xi )</td>
<td>0.093 (4-30)</td>
</tr>
<tr>
<td>Drain end depletion</td>
<td>( p )</td>
<td>0.292 (4-29)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Model Parameters</th>
<th>Curtice</th>
<th>TriQuint</th>
<th>Statz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance Parameter</td>
<td>( \beta )</td>
<td>7.11</td>
<td>7.11</td>
</tr>
<tr>
<td>Saturation Parameter</td>
<td>( \alpha )</td>
<td>2.57</td>
<td>–</td>
</tr>
<tr>
<td>Scale Parameter</td>
<td>( \gamma )</td>
<td>–</td>
<td>5.73</td>
</tr>
<tr>
<td>Doping tail Parameter</td>
<td>( b )</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
The current through the unsaturated portion of the channel is inversely proportional to its length so the transconductance parameter, $\beta$, is increased by $\frac{L}{L - \Delta L}$ which is modelled by the factor $(1 + \lambda V_{ds})$.

$$\frac{L}{L - \Delta L} = (1 + \lambda V_{ds}) \quad (4-41)$$

A problem exists with this expression because $\Delta L$, and hence $\lambda$, is a function of $V_{ds}$. However, the function is slow changing and a reasonable value can be obtained by setting $V_{ds} = 3W_{eo}$. The saturation potential, $V_{sat}$, is given by (3-3)†.

**Drain Feedback Parameter**

The drain feedback parameter is not easy to predict because it is dependent upon both the condition of the surface and the substrate. However, Hartgring [1982] presented an expression for the effective drain feedback capacitance

$$C_{dfb} = zC_{dfbo}V_{ds}^{-1/2}ln(L/L_o) \quad (4-42)$$

where $C_{dfbo} = 1.87 \times 10^{-12}$ F/cmV$^{-0.5}$ and $L_o = 1.7 \times 10^{-5}$ cm are empirical constants. The voltage dependence of this capacitance is due to the voltage dependence of the depletion region which separates the drain region from the undepleted part of the channel.

The change in channel charge density is

$$\Delta(q N_dazL) = C_{dfb}V_{ds} \quad (4-43)$$

This charge causes a change in depletion potential modelled by $\Delta V_{to} = \eta V_{ds}$ (3-6)†.

The change in depletion potential is

$$\eta V_{ds} = \Delta V_{to} = \frac{\Delta qN_daz^2}{2\varepsilon} = \frac{\Delta(qN_dazL)a}{2\varepsilon zL}$$

from (4-43)

using (4-42) gives

$$\eta V_{ds} = \frac{aC_{dfbo}ln(L/L_o)}{2\varepsilon L_\sqrt{W_{ds}}} V_{ds} \quad (4-44)$$

---

† $V_{sat} = \frac{\xi W_{eo}V_g}{V_g + \xi W_{eo}} \quad (3-3)$

† $V_{gs} \leftarrow V_g + \eta V_{ds} \quad (3-6)$
Experience has shown that $V_{ds} = 4W_{oo}$ gives a reasonable value for $\eta$:

$$\eta = \frac{\alpha C_{dibc} \ln(L/L_0)}{4 \varepsilon L \sqrt{W_{oo}}} \quad (4-45)$$

The high frequency drain feedback parameter is not easy to determine except through measurement. However, the author's experience has shown that setting ETA equal to ZETA is reasonable. The time constant can be set to 0.14 ms as suggested by Camacho-Penalosa and Aitchison [1985].

**Velocity Reduction Parameters**

The velocity reduction parameters are included to model the reduction in drain conductance which occurs when gate bias is increased. If this is considered as due to the reduction in electron velocity from its maximum velocity, $v_m$, to the saturated velocity, $v_s$, then the parameter $\kappa$ is set to the extent of this reduction.

$$\kappa = 1 - \frac{v_s}{v_m} \quad (4-46)$$

The rate of reduction, set by $\theta$ in the unified model, depends on the relation of the electric field to the drain-source potential.

Negative drain-source conductance is also attributed to local heating of the channel and this has been included in the TriQuint TOM model [McCaman and Smith 1989] with (2-36)$§$. This effect can be accommodated by adjusting $\theta$ and if necessary $\kappa$ to match.

**Source and Drain Ohmic Resistance**

Source and drain series resistances are composed of the ohmic contact resistance and resistance of the epi-layer separating the ohmic and Schottky contacts. Both the source and drain resistances are evaluated using the appropriate dimensions in (4-2)

$$R = R_a \frac{L_t}{z} \coth \left( \frac{d_s}{L_t} \right) + R_s \frac{d_s}{z} \left( \frac{2h_e}{h_e+a} \right) \quad (4-47)$$

$§$ $I_d = \frac{I_{ds}}{1 + \delta V_{ds} I_{ds}} \quad (2-36)$
Gate-Drain Junction Capacitance

The gate-drain junction capacitance is essentially due to the fringing of the depletion region into the drain contact region of the device. This depletion region is approximated by a quarter circle cross-section with radius equal to the drain end depletion depth (given by $d = \sqrt{\frac{V_{th} - V_{gs} + V_{ds}}{W_{oo}}}$ in section 2.3.2). This has a constant capacitance \[C_{gd} = \frac{\pi}{2} \varepsilon z\] \[(4-48)\]

When the drain-end is pinched off the fringe continues to spread towards the drain electrode but the cross section is no longer a complete quarter circle. The capacitance is calculated by Takada [1982] as an $\text{arctan}$ function. This is a slow changing function which can be approximated by a constant value:

$$C_{gd} = \varepsilon z \tan^{-1}\sqrt{\frac{W_{oo}}{V_{to} - V_{gd}}}$$

$$\approx \frac{\pi}{5} \varepsilon z \quad (4-49)$$

Since the Statz et al. [1987] capacitance model used in the unified model does not allow control over the variation in drain-gate capacitance, the fixed value is used for the model.

Gate-Source Junction Capacitance

The junction capacitance equation derived for the diode model (4-13) is applicable to the gate-source junction (using $L$ instead of $d_d$).

$$C_{gs} = Lz \sqrt{\frac{eqN_d}{2\phi_h}} + \frac{\pi}{2} \varepsilon z \quad (4-50)$$

The reduction in capacitance at pinch-off is controlled by the parameter $X_C$. This parameter is the ratio of the desired capacitance at pinch-off to the capacitance predicted by the inverse half-power law $\left(C_{gs}/\sqrt{1 - V/\phi_h}\right)$. When pinched off, the capacitance is due to fringing so the desired capacitance is equal to the drain-gate capacitance value (4-49).

$$X_C = \frac{C_{gd}}{C_{gs}} \sqrt{1 + W_{oo}/V_{to}} \quad (4-51)$$
**Gate Junction Potential**

The junction potential is set to the barrier height \( \phi_b \) as with the diode model.

**Doping Profile Parameter**

Unless the doping profile is known or measured data is available, the doping profile parameter, \( B \), should be set to 0.6 for a box profile (Refer section 3.2.1).

**Noise Parameters**

The development of noise models is beyond the scope of this work.

**MESFET Parasitic Capacitance**

The physical capacitances between the MESFET electrodes is calculated using (4-7) with the geometric parameter, \( k \), appropriately set. These are not included in the MESFET model but are added to the SPICE simulation as discrete elements.

**Example**

The unified model applied with the parameter equations in this chapter is compared with a measured device in Fig. 4.11. The 200 \( \mu \text{m} \times 1.5 \mu \text{m} \) device on chip M-2(3)H was used. The device nominal parameters listed in Table 4.1 were used to evaluate model parameters which are listed in Table 4.2. The agreement of the extracted model from nominal parameters with the actual device is very good. The Statz model is also shown in Fig. 4.11 with the same parameters used for Fig. 4.10 (listed in Table 4.1) except that the doping tail extending parameter, \( b \), is increased by 80% to improve the fit to measurement. This effectively sets \( b \) to match the saturation current at a gate-source bias lower than \( \phi_b \) used in (4-37).
Figure 4.11. Comparison of MESFET model using derived parameters listed in Tables 4.1 & 4.2 (solid lines) and measured device with the same physical parameter (diamond). The Statz et al. model is shown (dashed lines) using the parameters listed in Table 4.1 except $b$ is increased to 1.33 to improve the fit.

Table 4.2. Parameters for Unified MESFET Model.

<table>
<thead>
<tr>
<th>Model Parameters</th>
<th>Value</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pinch-off Potential</td>
<td>$V_{to}$</td>
<td>-3.75 V</td>
</tr>
<tr>
<td>Transconductance Parameter</td>
<td>$\beta$</td>
<td>27.1 mA/V^2</td>
</tr>
<tr>
<td>Doping Profile Parameter</td>
<td>$B$</td>
<td>0.6</td>
</tr>
<tr>
<td>Saturation Parameter</td>
<td>$\xi$</td>
<td>0.093</td>
</tr>
<tr>
<td>Drain Feedback Parameter</td>
<td>$\eta$</td>
<td>0.0499</td>
</tr>
<tr>
<td>Channel-Length Modulation Parm.</td>
<td>$\lambda$</td>
<td>78.6 mV^-1</td>
</tr>
<tr>
<td>Velocity Reduction Parameter</td>
<td>$\kappa$</td>
<td>0.359</td>
</tr>
</tbody>
</table>


**MESFET Summary**

The SPICE MESFET model parameters can be selected from the physical dimensions and properties of the device. The following list gives the parameter extraction equations for parameters of the unified model. Where applicable, a reference to the Curtice, TriQuint and Statz models is given.

1. **VTO** Threshold voltage is set by design
2. **BETA** Transconductance parameter, (4-39)
   - Curtice, TriQuint models, (4-34)
   - Statz Model, (4-36)
3. **XI** Saturation parameter, (4-30)
   - ALPHA Curtice, TriQuint models, (4-35)
   - Statz Model, (4-38)
4. **B** Doping profile parameter set by measurement
   - Statz Model, (4-37)
5. **LAMBDA** Channel-length modulation, (4-40) and (4-41)
   - Curtice, TriQuint, Statz models need drain feedback included
6. **ETA** Drain feedback, (4-45)
7. **ZETA** AC drain feedback, set initially equal to ETA
8. **RD** Parasitic drain resistance, (4-47)
9. **RS** Parasitic source resistance, (4-47)
10. **CGS** Junction and fringe components, (4-50)
11. **CGD** Fringe component, (4-49)
   - Curtice, TriQuint models, set equal to CGS
12. **IS** Richardson equation for the metal, (4-18)
13. **PB** Built in potential set to diode VJ, (4-12)
14. **XC** Capacitance Pinch-off parameter, (4-51)
15. **KAPPA** Current reduction, (4-46)
16. **THETA** Current reduction rate, at default or fit measurements
17. **TAU** Drain feedback time constant, set to 0.14 ms
18. **KF** Default at zero, noise not considered
19. **AF** Default at one, noise not considered
20. **FC** Default at 0.5
21. **CMOD** Default at 2 to use Statz capacitance model
4.5 Fundamental Parameters

The simulation model parameters have been derived from the fundamental physical properties of the devices and fabrication process. This allows the extraction of circuit models from knowledge of the device dimensions or layout. In addition, the effects of the fabrication variation can be predicted. The fundamental parameters used are classified in Table 4.3 into three categories: material dependent, process dependent and design dependent.

**Material Parameters**

The crystal and electron transport properties of the material are not affected by subsequent fabrication steps. However, they are affected by design parameters such as the choice of nominal doping level and operating temperature. The equations which predict these influences are listed in Table 4.3.

**Process Parameters**

The process parameters are dictated by the capabilities of the fabrication process and are independent of the type of device constructed with the process. Process changes affect the quality of Schottky junctions and ohmic contacts. The Schottky metal chosen is significant and its properties are required to predict Schottky barrier heights and diode ideality factor. Alloyed ohmic connections vary with the contact geometry so measured parameters are used to predict contact resistance. Also, the electrode spacing varies with mask alignment tolerances.

**Design Parameters**

Devices used for a particular circuit can be tailored to the application by setting the design parameters. Parasitic resistances and capacitances are affected by the device geometries. MESFET pinch-off potential, for example, is adjusted by setting the channel depth. Trade-offs with power and circuit density go with the selection of these parameters.
4.5.1 Variation of Parameters

Those parameters in Table 4.3 which are considered constant are relative permittivity, $\varepsilon_r$, the Schottky metal work function, $\phi_m$, relative electron masses in GaAs and the Schottky metal, $m^*/m$ and $m_0/m$, and breakdown field, $E_b$. The device electrode dimensions, $d_d$, $d_s$, and $L$ do not vary significantly and are also considered constant (unlike electrode spacing).

The variation of seven of the parameters in Table 4.3 is a necessary and sufficient knowledge in order to determine the variation of device and circuit characteristics. These parameters are:

- temperature, $T$
- measured process dependent resistance parameters, $R_a$ and $R_c$
- nominal doping level, $N_d$
- nominal channel depth, $a$
- variation in electrode spacings, $d_e$, $d_s$.

The remaining parameters are dependent upon these parameters and a set of proportional relations can be established:

The density of conduction states is dependent on temperature.

From (2-7) \[ N_c \propto T^{32} . \] (4-52)

Mobility is dependent on temperature and doping level

From (2-6) \[ \mu \propto T^{-1} N_d^{-0.151} \] (4-53)

The electron velocity parameters, $E_m$, $v_m$, and $v_s$, are functions of mobility. The author’s graphical analysis of (4-27) and (4-28) has given their dependence on mobility and (4-53) gives their dependence on temperature and doping level:

\[ v_m \propto \mu^{0.8} \propto T^{0.8} N_d^{-0.121} \] (4-54)
\[ E_m \propto \mu^{-0.25} \propto T^{0.25} N_d^{0.038} . \] (4-55)

The barrier height, $\phi_b$, is dependent on temperature and doping level as given by equation (4-12). Its dependence on density of conduction states can be traced to temperature with (4-52).
The ohmic contact transfer length is a function only of the resistance parameters, $R_a$ and $R_c$.

The dependency relations determined in this section can also be applied to determine the variation measured characteristics. For example, consider the measured mobility $\mu_m$ in a sample of material with doping $N_m$ at a temperature $T_m$. The mobility at temperature $T$ in material with doping $N_d$ can be determined from (4-53) as $\mu = \mu_m (T_m/T)^{0.151} (N_m/N_d)^{0.151}$. This illustrates a benefit of the implicit dependency on fundamental parameters in the extraction equations developed in this chapter.

### Table 4.3. Fundamental Fabrication Process Parameters.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Default</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m^*/m$</td>
<td>0.068</td>
<td>—</td>
<td>Relative electron mass in GaAs</td>
</tr>
<tr>
<td>$N_C$</td>
<td>(2-7)</td>
<td>$m^{-3}$</td>
<td>Density of conduction states</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>13.1</td>
<td>—</td>
<td>Relative permittivity</td>
</tr>
<tr>
<td>$\mu$</td>
<td>(2-6)</td>
<td>$m^2/Vs$</td>
<td>Low field drift mobility</td>
</tr>
<tr>
<td>$E_m$</td>
<td>(4-28)</td>
<td>$V/m$</td>
<td>Maximum electron velocity field</td>
</tr>
<tr>
<td>$v_m$</td>
<td>(4-27)</td>
<td>$m/s$</td>
<td>Maximum electron velocity</td>
</tr>
<tr>
<td>$v_s$</td>
<td>(2-5)</td>
<td>$m/s$</td>
<td>Saturated electron velocity</td>
</tr>
<tr>
<td>$E_b$</td>
<td>$4 \times 10^5$</td>
<td>$V/m$</td>
<td>Breakdown Field</td>
</tr>
<tr>
<td>$m^*/m$</td>
<td>1.2</td>
<td>—</td>
<td>Rel. electron mass in Schottky metal</td>
</tr>
<tr>
<td>$\phi_m$</td>
<td>3.38</td>
<td>$eV$</td>
<td>Work function of Schottky metal</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>(4-12)</td>
<td>$V$</td>
<td>Schottky barrier height</td>
</tr>
<tr>
<td>$R_S$</td>
<td>150</td>
<td>$\Omega/sq$</td>
<td>Epi-layer sheet resistance</td>
</tr>
<tr>
<td>$R_a$</td>
<td>15</td>
<td>$\Omega/sq$</td>
<td>Ohmic alloy sheet resistance</td>
</tr>
<tr>
<td>$R_C$</td>
<td>$3000$</td>
<td>$\Omega.m^2$</td>
<td>Metal to alloy contact resistance</td>
</tr>
<tr>
<td>$L_t$</td>
<td>(4-1)</td>
<td>$m$</td>
<td>Ohmic contact transfer length</td>
</tr>
<tr>
<td>$d_e$</td>
<td>0.5</td>
<td>$\mu m$</td>
<td>Gate-drain and gate-source spacing</td>
</tr>
<tr>
<td>$d_s$</td>
<td>1.5</td>
<td>$\mu m$</td>
<td>Diode electrode spacing</td>
</tr>
<tr>
<td>$N_d$</td>
<td>$2 \times 10^{17}$</td>
<td>$m^{-3}$</td>
<td>Nominal Doping Level</td>
</tr>
<tr>
<td>$L$</td>
<td>1</td>
<td>$m$</td>
<td>MESFET gate length</td>
</tr>
<tr>
<td>$a$</td>
<td>(2-23)</td>
<td>$Å$</td>
<td>MESFET channel depth</td>
</tr>
<tr>
<td>$d_d$</td>
<td>2.5</td>
<td>$\mu m$</td>
<td>Diode Schottky metal length</td>
</tr>
<tr>
<td>$d_o$</td>
<td>5</td>
<td>$\mu m$</td>
<td>Ohmic contact physical length</td>
</tr>
<tr>
<td>$T$</td>
<td>310</td>
<td>$K$</td>
<td>Temperature</td>
</tr>
</tbody>
</table>
4.6 Summary

This chapter has described how the electrical properties and physical details of the devices are used to derive parameters required for SPICE models.

Resistance and capacitance parameters have been considered. A description of ohmic contact resistance has been developed. The transfer length is identified as a practical design limit on the contact’s physical length. Improved methods for extracting the equivalent lumped capacitance elements between metal wiring and to ground have been developed. These passive components are included in active device models as parasitic elements.

Diode dc and ac model parameters are determined from the device physical properties. Temperature parameters are adapted for GaAs. The Richardson-Dushmann equation is used to determine reverse leakage current. In the forward bias mode the Richardson constant is adjusted for the electron mass in the semiconductor. The electron mass in the metal is used for the reverse bias case which is a correction to accepted theory. This gives an expression which predicts an emission co-efficient greater than unity as in real devices. Also, a suitable model of diode planar effects using two ideal diodes in series is applied. A maximum device dimension design rule which avoids planar effects has been developed.

MESFET parameters are selected so that the zero bias saturation current and the drain resistance at zero drain voltage are the same as predicted by the Pucel et al. [1975] model. Expressions for the second-order effects of channel-length modulation, drain feedback and velocity reduction are described for the unified MESFET model. The gate-drain fringing capacitance and gate-source junction capacitance are derived in the same way as for the diode model.

Deriving model parameters from the physical properties of the devices facilitates the extraction of circuit models from device layouts as has been demonstrated with measured devices. This also allows study of effects of fabrication variations.

Physical properties have been classified into three categories: material, process and design dependent. From these, the basic properties that must be considered to predict variation of device and circuit characteristics have been identified. The appropriate variation of the device characteristics, implicit in the extraction equations, were given.
4.6.1 Chapter 4 References

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5 Design of Basic Logic Gate

5.1 Introduction

The speed capability of a GaAs logic gate is often determined by the manufacturing process. At the same time there is a necessary trade between speed and some other parameter such as size or power dissipation. However, within the process limitation it is possible to design the gate circuit so that good logic and maximum speed are extracted from the technology.

A design procedure is developed in this chapter which uses a simple piecewise linear transistor model for selecting the relative sizes of the transistor elements in a logic gate to give minimum switching time for a particular load. The process parameters identified in section 4.5 form a basis for extending the procedure to accommodate temperature variation and fabrication tolerances. The analysis clearly identifies the dependency on loading of both buffered and unbuffered topologies. It is also confirmed that the transit time under the gate is an intrinsic factor which can be used as a figure of merit for developing the fabrication process. In addition, a result of this study is a new logic family called Saturated Buffered FET logic (SBFL) which achieves reduced power, reduced circuit area, better fan-out performance and better speed than buffered FET logic.

The gate design procedure is easily automated and forms the core of a software
package, described in Chapter 7, which produces a template gate. This template is the basis for the automatic generation of a standard logic gate library.

In the following section, 5.2, a simple piecewise linear model of a MESFET is presented. This model is used to calculate the relative sizes of transistors in the logic gate so that a specified dc logic swing is achieved. The design procedure is completed in section 5.3 by using speed performance as the basis for selecting buffer stage size and fan-out loading. Section 5.4 presents the SBFL logic family and explains its operation. Section 5.5 extends the design procedure to accommodate variation in device parameters. An algorithm for producing extreme cases is presented. Finally, section 5.6 discusses the automation of the design procedure and gives an example.

5.2 DC Specification

The various documented depletion mode logic families (described in chapter 2) fall into two categories: buffered and unbuffered. Unbuffered FET logic consists of an inverting switch transistor with drain load followed directly by a level-shift network and pull-down transistor. Buffered logic adds a source follower between the inverter and level-shift devices to improve its driving capability.

Logic functions are implemented with combinations of single-gate and dual-gate switch transistors. Alternatively, logic can be performed by a network of level-shift diodes as in SDFL.

5.2.1 Device Characteristics

The design of logic gates is simplified by using a piecewise linear MESFET model as shown in Fig. 5.1. A single model is sufficient because all devices in the depletion mode circuit differ only in width. The model uses six parameters to define straight line segments as the device characteristics for a one unit wide device. The zero-gate-bias saturated drain current, \( I_{\text{dss}} \), the transconductance, \( g_m \), the near-pinch-off transconductance, \( g_x \), and the effective near-pinch-off zero-gate-bias saturated current, \( I_x \), define the relation between the saturated drain current and the gate-source bias. The drain-source potential of the saturation knee is defined by the zero-current saturation potential, \( V_s \), and the effective conductance of saturation potential, \( G_s \). For convenience, the effective gate-source pinch-off potential, \( V_{po} \), and the near-pinch-off turn-off potential, \( V_{to} \), are defined. These are equal to \(-I_{\text{dss}}/g_m\) and \(-I_x/g_x\) respectively. This piecewise linear approximation is quite good for the short channel MESFET devices because velocity
saturation effects give a sharper saturation knee. A long channel device has a more gradual saturation and would require a more detailed model.

5.2.2 Design Equations

A suitable starting point for the design of a digital logic family is the dc specification of the logic. The most important consideration is providing adequate noise immunity by having a large and symmetrical logic swing. This must be balanced against the switching time and energy advantages of a small logic swing.

Consider the inverter stage in BFL, shown in Fig. 5.2, driven by high and low logic levels, $V_h$ and $V_l$ respectively. The corresponding potentials at the output of an inverting logic gate, which are the same as those applied to the input of the next logic gate, can be evaluated in terms of the voltage drops across the devices in the gate. A logic high output is set by the positive power supply potential, $V_{dd}$, less the potential drop across the source follower and diode chain, $V_{ds, sf} + V_d$. The output logic threshold, $V_{mid}$, occurs when the switch transistor and pull-up draw the same current. The logic low at the output is nominally the potential at the drain of the switch device shifted by the diode chain but can be limited by the negative supply potential, $V_{ss}$, through the pull-down
transistor. The gate-source potential of the source follower is assumed to be zero. These relationships are described by the following equations.

\[
V_h = V_{dd} - V_{ds sf} - V_d \quad (5-1)
\]

\[
V_l = \max\{V_{ds sw} - V_d, V_{ss} + V_{ds pd}\} \quad (5-2)
\]

Rearranging these establishes the required power supplies:

\[
V_{ss} \leq V_{ds sw} - V_{ds pd} - V_d \quad (5-3)
\]

\[
V_{dd} \geq V_h - V_l + V_{ds sf} + V_{ds sw} \quad (5-4)
\]

To avoid excessive Schottky junction current in the switch of the next logic gate the maximum high logic level must be limited to the built-in potential, \(\phi_b\), of the gate: (In practice, a fraction, say half, of \(\phi_b\) has proven useful to leave a margin for process variation.)

\[
V_d \geq V_{dd} - V_{ds sf} - \phi_b \quad (5-5)
\]

For maximum noise immunity with minimum logic swing, it is desirable to have symmetry about the logic threshold:

\[
V_h - V_{mid} = V_{mid} - V_l \quad (5-6)
\]

The relative width of the switch and pull-up transistors is adjusted so that the bias required to give the switch the same current as the pull-up is half-way between the two logic levels. This satisfies (5-6). The current through the transistors is proportional to the product of their width and gate-source bias, so the condition is met when

\[
z_{pu}(0 - V_{po}) = z_{sw}\left(\frac{V_h + V_l}{2} - V_{po}\right)
\]

(Note \(V_{po}\) is a negative quantity)

which gives

\[
\frac{z_{pu}}{z_{sw}} = 1 - \frac{V_h + V_l}{2V_{po}} \quad (5-7)
\]

The drain source potential of the switch transistor with a high logic input is determined by geometric analysis of its characteristics (Fig. 5.1) with the pull-up charac-

\[\begin{align*}
V_l &\geq V_{ss} + V_{ds pd} \quad \text{and} \quad V_l \geq V_{ds sw} - V_d \\
\therefore \quad V_{ss} &\leq V_l - V_{ds pd} \leq V_{ds sw} - V_d - V_{ds pd} \\
\text{From (5-1)} \quad V_{dd} &= V_h + V_{ds sf} + V_d \quad \text{and from (5-2)} \quad V_l \geq V_{ds sw} - V_d \\
\therefore \quad V_{dd} &\geq V_h + V_{ds sf} + V_{ds sw} - V_l
\end{align*}\]
teristic as a load line. It is assumed that the switch is not operating in the 'near-pinch-off' region so its saturated drain current is $I_{ds} = I_{dss} + g_m V_h$. Examination of Fig. 5.1 shows that the switch's saturation knee follows a locus described by

$$I_{ds} = I_{dss} + g_m V_h$$

so with the high logic input the saturation knee is at

$$V_{ds} = (I_{dss} + g_m V_h) G_s + V_s.$$  

Since the pull-up transistor limits the actual operating current to $z_{pu} I_{dss}$ the switch operates in the linear mode. Therefore, the drain-source potential of the switch is less than the saturation knee potential:

$$V_{ds,sw} = \frac{z_{pu}}{z_{sw}} I_{dss} + g_m V_h \left( \frac{I_{dss}}{G_s} + \frac{g_m V_h}{G_s} + V_s \right)$$  \hspace{1cm} (5-8)

The potential across the pull-down when the inverter input is high and across the pull-up transistor when the input is low can be similarly evaluated. In both cases the same form as (5-8) arises with the gate-source potential of each at zero ($V_h = 0$ in (5-8)).

In the case of the pull-down transistor, its width and drain current are assumed to be the same as the source follower. (This assumption is substantiated in section 5.3.2.) This gives a drain-source potential when the inverter input is high of

$$V_{ds, pd} = \frac{I_{dss}}{G_s} + V_s.$$  \hspace{1cm} (5-9)

Figure 5.2. The basic BFL inverter. Device sizes and power supply values were determined with the design equations presented here. The source follower width is set to give maximum speed with a load of 4 of the same BFL gates.
The expression for the drain-source potential of the pull-up transistor when the input is low accounts for the possibility of the switch transistor operating in the ‘near-pinch-off’ region: (again with the same form as (5-8))

\[
V_{ds\,pu} = \frac{z_{sw}}{z_{pu}} \max \left( 0, \frac{I_x + g_s V_l, I_{dss} + g_m V_{l1}}{I_{dss} \left( G_s + V_s \right)} \right) \tag{5-10}
\]

The total drain-source potential of the source follower is a function of the drain-source potential of the pull-up transistor.

The drain source potential of the source follower is described by an expression with the same form as (5-8) using the width of the pull-down \(z_{pd}\) instead of \(z_{pu}\) and the source follower \(z_{sf}\) instead of \(z_{sw}\). The gate-source bias of the source follower is the difference between the drain-source potentials of the source follower and the pull-up. It can be assumed that the widths of the pull-up transistor and the source follower are the same.

\[
V_{ds\,sf} = \frac{I_{dss}}{I_{dss} + g_m (V_{ds\,sf} - V_{ds\,pu})} \left( \frac{I_{dss}}{G_s} + g_m (V_{ds\,sf} - V_{ds\,pu}) + V_s \right) \]

The solution to this quadratic equation in \(V_{ds\,sf}\) is

\[
V_{ds\,sf} = \frac{1}{2} \left\{ V_{ds\,pu} + \frac{I_{dss}}{G_s} - \frac{I_{dss}}{g_m} \pm \sqrt{ \left( V_{ds\,pu} + \frac{I_{dss}}{G_s} - \frac{I_{dss}}{g_m} \right)^2 + 4 \frac{I_{dss}}{g_m} \left( \frac{I_{dss}}{g_m} - V_{ds\,pu} \right) + V_s } \right\} \ 
\]

\...(5-11a)

The application of (5-1) to (5-5) to unbuffered logic with no source follower is facilitated by using the drain-source potential of the pull-up instead of the source follower:

\[
V_{ds\,sf} = V_{ds\,pu} \tag{5-11b}
\]

**Solving the Design Equations**

The use of (5-1) to (5-11) is as follows: Firstly, starting with an initial required logic swing, \(V_h - V_l\), the values of the drain-source potentials of the devices are estimated using (5-8) to (5-11) with \(V_h\) set to \(\frac{V_h}{2}\). Secondly, these estimates and (5-3), (5-4) and (5-5) are used to determine the necessary power rails and diode chain potential. The power supply values can be rounded to a nominal value. Thirdly, (5-1), (5-2) and (5-7) to (5-11) are solved iteratively to give a self-consistent solution for the logic levels. This
system will not converge if the required logic swing is not obtainable with the devices. For example, a logic swing much greater than the pinch-off voltage is not easy to produce because the switch transistor cannot respond evenly over the entire logic swing.

This system has been programmed into the GaAsSPICE software described in Chapter 7 and it is useful for performing a “What if?” analysis with various initial logic swings. With this tool it is possible to decide rapidly upon suitable logic and power supply values to suit the available devices.

5.2.3 Fan-In and Fan-Out Loading

If there are \( f_{in} \) switch transistors in the inverter stage, one of them can switch the gate when the others are off. The off switches have a low logic input which does not imply that they have zero drain current because the low logic level can be greater than the pinch off potential. Thus the width of the pull-up transistor must be extended to offset any fan-in loading current through the off switches. Also, in unbuffered logic with a fan-out \( f_{out} \) the pull-up must be extended to offset the current drawn by the pull-down transistors.

\[
z_{pu \ total}I_{dss} = z_{pu}I_{dss} + (f_{in} - 1)z_{sw}(I_{x}x_{g}V_{l}) + f_{out}z_{pd}I_{dss}
\]

(5-12)

where \( f_{out} = 0 \) in buffered logic.

The extra width added to the pull-up transistor is not considered in the design equations because the extra current is always balanced by the fan-in and fan-out loading and therefore plays no part in the switching action. Of course, the extra width does increase the power consumption of the gate.

5.2.4 Dual-Gate Switches

The width of the dual-gate switch transistor, \( z_{an} \), must be set to provide NAND inputs which are compatible with the single-gate NOR input given by the design equations. The difficulty with dual-gate transistors is that each input has a different logic threshold. This reduces noise margin because at least one input must have a threshold which is not half-way between the logic levels. However, this degradation is accepted for convenience and circuit simplicity.

Dual-gate transistors are modelled as two series single-gate devices. The logic threshold of the lower gate, \( V_{lower} \), is determined assuming the upper device is turned on. The lower logic threshold is the input potential required so that the lower transistor
draws a current equal to the pull-up transistor’s current.

\[ z_{pu} I_{dss} = z_{an} g_m (V_{lower} - V_{po}) \]

\[ \therefore \quad V_{lower} = \frac{z_{pu} I_{dss}}{z_{an} g_m} + V_{po} \quad (5-13) \]

If the lower device is turned on by a high logic level the upper gate logic threshold, \( V_{upper} \), is the gate potential required for it to draw a current equal to the pull-up transistor’s current. The drain-source voltage across the lower device is added to the upper’s gate-source potential.

\[ z_{pu} I_{dss} = z_{an} g_m \left( V_{upper} - V_{po} - \frac{z_{pu} I_{dss}}{z_{an} g_m} + \frac{V_s}{1 - V_h/V_{po}} \right) \]

\[ \therefore \quad V_{upper} = \frac{z_{pu} \left( I_{dss} + \frac{V_s}{1 - V_h/V_{po}} + \frac{I_{dss} g_m}{g} \right)}{z_{an}} + V_{po} \quad (5-14) \]

The difference between these logic thresholds is accommodated by setting their average to the logic threshold of the single-gate input.

\[ \frac{V_h + V_l}{2} = \frac{V_{lower} + V_{upper}}{2} \]

\[ \therefore \quad V_h + V_l = \frac{z_{pu} I_{dss}}{z_{an} g_m} + V_{po} + \frac{z_{pu} I_{dss}}{z_{an} g_m} \left( \frac{I_{dss} g_m}{g_s} + \frac{V_s}{1 - V_h/V_{po}} \right) + V_{po} \]

\[ \therefore \quad \frac{z_{an}}{z_{pu}} = \frac{I_{dss} (1/G_s + 2/g_m) + V_s (1 - V_h/V_{po})}{V_h + V_l - 2V_{po}} \quad (5-15) \]

The difference between the logic thresholds is

\[ V_{upper} - V_{lower} = \frac{z_{pu} \left( I_{dss} + \frac{V_s}{1 - V_h/V_{po}} + \frac{I_{dss} g_m}{g} \right)}{z_{an}} + V_{po} - \frac{z_{pu} I_{dss}}{z_{an} g_m} - V_{po} \]

\[ = \frac{z_{pu} \left( I_{dss} + \frac{V_s}{1 - V_h/V_{po}} \right)}{z_{an}} \quad (5-16) \]

With the device shown in Fig 5.1 and a logic swing between \(-2.0\) and \(+0.25\) V the logic threshold difference is 345 mV (about 15% of the logic swing). The use of three or more series FET’s is not practical because the variation in logic threshold between each input is too large.
5.2.5 Diode Chain Specification

It is necessary to use the correct number of diodes so that a reliable level-shift is obtained. If there are too few diodes, they must be narrow and the voltage drop is dominated by their series resistance which has a poor process tolerance. On the other hand a large number will occupy a larger area.

A reasonable rule-of-thumb is to set the diode width so that the change in diode potential drop caused by process changes of resistance is approximately the same as the change over the expected operating temperature range. The following implicit equation satisfies this condition for the current supplied by the pull-down transistor.

\[ \Delta V_d = \Delta R_s \frac{z_{pd}I_{dss}}{z_d} + \Delta T \frac{Nk}{q} \ln \left( \frac{z_{pd}I_{dss}}{z_dI_s} \right) \]

so let

\[ \frac{z_{pd}I_{dss}}{z_d} \Delta R_s = \frac{Nk\Delta T}{q} \ln \left( \frac{z_{pd}I_{dss}}{z_dI_s} \right) \] (5-17)

The number of diodes necessary to give the required voltage drop is easily calculated.

\[ \eta = \frac{V_d}{\frac{NkT}{q} \ln \left( \frac{z_{pd}I_{dss}}{z_dI_s} \right) \frac{z_{pd}I_{dss}R_s}{z_d}} \] (5-18)

This must be rounded to the nearest integer then the width of the diodes can be reset to give the correct voltage drop.

5.3 AC Optimization

It still remains to define the size of the level-shift devices relative to that of the inverter stage. This relation determines the fan-out capability of the gate and can be optimised for maximum speed.

5.3.1 Fall-Time

The inverter stage must charge the gate capacitance of the source follower before that can in turn charge the output. When the switch transistor is turned on the available charging current is offset by the current through the pull-up transistor. In terms of
the piecewise linear model (Fig. 5.1) the relative currents are proportional to the device widths:

\[ I_{\text{available}} = z_{sw}(I_{dss} + g_m V_h) - z_{pu} I_{dss} \] 

(5-19)

Substituting \(-g_m V_{po} = I_{dss}\) and (5-7)† into (5-19) gives the available current:

\[ I_{\text{available}} = z_{sw} g_m \frac{V_h - V_l}{2} \] 

(5-20)

The charge that must be delivered to the source follower’s gate-source junction is the product of the junction capacitance, \(z_{sf} C_{gs}\), and the effective voltage change of the gate-source junction which occurs at the beginning of the falling transition, \(\Delta V_{sfh}\). The fall-time of the step response to 1 neper can be estimated assuming the constant charging current given by (5-20) (1 neper = \(\frac{1}{1.58}\)):

\[ \tau_{f1} = \frac{1}{1.58} \frac{C \Delta V}{I_{\text{available}}} \]

\[ = \frac{2 z_{sf} C_{gs} \Delta V_{sfh}}{1.58 z_{sw} g_m (V_h - V_l)} \] 

(5-21)

The buffer chain consists of the source follower, level shifting diodes and the pull-down transistor. In general the fall-time is determined by the size of the pull-down transistor. When the source follower is switched-off the current available from the pull-down transistor will be \(z_{pd} g_m V_{po}\). Assuming that the load consists of \(f\) switch transistors, the fall-time to 1 neper is given by

\[ \tau_{f2} = \frac{1}{1.58} \frac{C \Delta V}{I_{\text{available}}} \]

\[ = \frac{f C_{gs} z_{sw} (V_h - V_l)}{1.58 z_{pd} g_m V_{po}} \] 

(5-22)

The overall delay of the circuit is the sum of the step response delays of the inverter and buffer chain (5-21) and (5-22). Also, a correction factor \(K\) (not necessarily constant) is required because the source follower is fed with the step response of the inverter rather than a rectangular pulse.

\[ \tau_f = K \left( \frac{2 z_{sf} C_{gs} \Delta V_{sfh}}{1.58 z_{sw} g_m (V_h - V_l)} + \frac{f C_{gs} z_{sw} (V_h - V_l)}{1.58 z_{pd} g_m V_{po}} \right) \] 

(5-23)

\[ \frac{z_{sw}}{z_{vw}} = 1 - \frac{V_h - V_l}{2V_{po}} \] 

(5-7)
The optimum ratio of transistor widths for minimum fall-time occurs when the two impulse delays are equal, in which case \( K = 1.08 \). By equating (5-21) and (5-22) the transistor ratios can be optimised for a nominal fan-out, \( F \). The total fall time is a linear function of the actual fan-out, \( f \).

\[
\frac{z_{af}}{z_{sw}} = (V_h - V_l) \sqrt{\frac{F z_{sf}}{2 \Delta V_{sh} |V_{po}| z_{pd}}} \tag{5-24}
\]

(5-24) into (5-23) gives

\[
\tau_f = \left(1 + \frac{f}{F}\right) \frac{0.965 C_{gs}}{g_m} \sqrt{\frac{F \Delta V_{sh} z_{sf}}{|V_{po}| z_{pd}}} \tag{5-25}
\]

### 5.3.2 Rise-Time.

When the switch transistor has a high logic input the available charging current is the current through the pull-up transistor less the current through the switch transistor:

\[
I_{\text{available}} = z_{pu} \left( I_{dss} - z_{sw} g_m (V_l - V_{po}) \right)
\]

\[
= -z_{pu} g_m V_{po} - z_{sw} g_m (V_l - V_{po}) \tag{5-26}
\]

The rise-time is calculated with (5-26), (5-7)†, and by assuming the capacitance to be charged is \( z_{sf} C_{gs} \) and the effective voltage change of the gate-source junction is \( \Delta V_{sfl} \):

\[
\tau_{r1} = \frac{1}{1.58} \frac{C \Delta V}{I_{\text{available}}}
\]

\[
= \frac{2 z_{af} C_{gs} \Delta V_{sfl}}{1.58 z_{sw} g_m (V_h - V_l)} \tag{5-27}
\]

The buffer rise-time is determined by the current through the source follower less that through the pull-down transistor. When the source follower gate-source junction is forward biased to the built-in potential the charging current to the output node is \( z_{sf} g_m (\Phi_n - V_{po}) - z_{pd} g_m (-V_{po}) \). During the initial part of the rising transition the switch transistor loads are either nearly or actually pinched off and their gate-source

---

\( \S \) The total impulse delay of two `black boxes’ with the same RC time constant connected in series is 2\( \times 0.32 \) time constants. This has been checked by the author through simulation.

\( \dagger \) \[
\frac{z_{pu}}{z_{sw}} = 1 - \frac{V_h + V_l}{2V_{po}} \tag{5-7}
\]
capacitance is lower than (say a factor $k$) the zero-bias value because of depletion limiting\footnote{The reduction in junction capacitance is caused by the complete depletion of the channel region so that charge movement is restricted to fringing at the drain and source ends of the channel. A model and parameters for this effect have been developed in chapters 3 and 4.}.

$$
\tau_r^2 = \frac{1}{1.58} \frac{C \Delta V}{I_{\text{available}}}
= \frac{f \kappa C_{gs} z_{sw} (V_h-V_l)}{1.58 g_m \left( z_{sf} (\Phi_b-V_{po}) + z_{pd} V_{po} \right)}
$$

(5-28)

The total rise-time is the sum of (5-27) and (5-28).

$$
\tau_r = K \left( \frac{2 z_{sf} C_{gs} \Delta V_{sfl}}{1.58 z_{sw} g_m (V_h-V_l)} \right) + \frac{f \kappa C_{gs} z_{sw} (V_h-V_l)}{1.58 g_m \left( z_{sf} (\Phi_b-V_{po}) + z_{pd} V_{po} \right)}
$$

(5-29)

As with the fall-time calculation the optimum ratio of transistor widths for minimum fall-time occurs when the impulse delays for the switch and buffer stages are equal. Equating (5-27) and (5-28) gives:

$$
\frac{z_{sf}}{z_{sw}} = \frac{(V_h-V_l) \sqrt{kF^2}}{2 \Delta V_{sfl} (\Phi_b-V_{po} + V_{po} z_{pd}/z_{sf})}
$$

(5-30)

Equating (5-30) and (5-24) finds the pull-down width, $z_{pd}$, which gives optimum rise and fall time.

$$
\frac{z_{sf}}{z_{pd}} = \frac{1 + \kappa \Delta V_{sfl} / \Delta V_{sfl}}{1 - \Phi_b / V_{po}}
$$

(5-31)

Generally this will set the source follower width greater than the pull-down width. However, then when the output is low the source follower’s gate-source junction will have a negative bias which defeats the level shifting function of the buffer stage. This is avoided by making the source follower’s size equal to that of the pull-down transistor which does not significantly degrade the speed of the gate.

Setting $z_{pd} = z_{sf}$ gives final expressions for the rise- and fall-times of the gate:

From (5-24)

$$
\frac{z_{sf}}{z_{sw}} = (V_h-V_l) \sqrt{\frac{F}{2 \Delta V_{sfl} |V_{po}|}}
$$

(5-32)

from (5-25)

$$
\tau_f = \left(1 + \frac{I}{F} \right) \frac{0.965 C_{gs}}{g_m} \sqrt{\frac{F \Delta V_{sfl}}{|V_{po}|}}
$$

(5-33)
(5-32) into (5-29) gives
\[
\tau_t = \left( \frac{\Delta V_{th}}{\Delta V_{sh}} + \frac{L}{F} \frac{\kappa}{\phi_b} \left| V_{po} \right| \right) 0.965 C_{gs} g_m \sqrt{\frac{F \Delta V_{sh}}{V_{po}}} \tag{5-34}
\]

As expected, the form of (5-33) and (5-34) represents a finite no-load delay and an incremental delay proportional to the fan-out loading.

### 5.3.3 Transit-Time as Figure of Merit

The common factor in the timing equations (5-33) and (5-34) is the ratio of junction capacitance to transconductance which is the transit time under the gate.

\[
\tau_t = \frac{C_{gs}}{g_m} \tag{5-35}
\]

It is clear that this time must be minimized in order to increase the speed of the circuit. Thus a study of this parameter can indicate which facets of the fabrication process should be changed to achieve better speed.

Because of the curvature of the MESFET transconductance characteristic the transconductance of the intrinsic transistor is greater than the ratio of its maximum current (4-33)† to its depletion potential.

\[
g_m > \frac{I_{\text{max}}}{W_{\text{co}}} = \frac{v_m q N_d a z (1-p)}{W_{\text{co}}} \frac{L}{L-L_{\text{sat}}} \tag{5-36}
\]

An upper limit for the transit time of a device (5-35) can be determined with (5-36) and the gate junction capacitance (4-49)§.

\[
\tau_t < \varepsilon z \frac{L}{a} \sqrt{\frac{W_{\text{co}}}{\phi_b}} \frac{W_{\text{co}}}{W_{\text{co}}} \frac{1}{2(1-p)} \frac{L-L_{\text{sat}}}{L} \tag{5-37}
\]

This expression for transit time is, as expected, the ratio of distance to velocity with a scaling parameter which is required to account for the non-ideal shape of charge distribution and the velocity under the gate. Including the source parasitic resistance,

\[
I_{\text{max}} = \frac{v_m q N_d a z (1-p)}{L-L_{\text{sat}}} \frac{L}{L-L_{\text{sat}}} \tag{4-33}
\]

\[
C_{\text{Jo}} = L z \sqrt{\frac{q N_d}{2 \phi_b}} + \frac{\pi}{2} \varepsilon z \tag{4-49}
\]
$R_{ss}$ decreases the transconductance, $g_m$, by a factor $(1+g_mR_{ss})$. The transit time is then increased by the same factor.

A smaller transit time for high speed switching devices is continually sought by decreasing the source resistance and gate length through process improvements. The transit time can also be reduced by decreasing the depletion potential in the circuit. The trade-off with reducing the depletion potential is that the logic swing is also reduced and so the noise margin is reduced. The smallest useful depletion potential is also limited so that its variation due to fabrication process is kept to within 5% [Eden 1982]. Note that the analysis above is the result of studying a depletion mode logic gate so $W_m$ must be greater than the built-in potential.

### 5.3.4 Example

The MESFET characteristics shown in Fig. 5.1 are typical of those used in digital applications and they are used here to verify the timing equations (5-33) and (5-34). The piecewise linear model parameters and capacitance values needed for the timing equations are $g_m = 160 \mu A/\mu m$, $V_{po} = -1.22 V$, $C_{gs} = 1.6 fF/\mu m$. The BFL gate shown in Fig. 5.2 was designed for this MESFET with the design equations (5-1) to (5-12). The logic levels are given by the design equations and simulated as $V_h = 0.25 V$ and $V_l = -2.0 V$.

The SPICE simulation shown in Fig 5.3 is of the falling transitions for BFL gates with ratios of source follower to switch transistor ranging from 0.83 to 5. A fan-out load consisting of four BFL gates is used for each gate. The factor $K$ in (5-23) accounts for the non-rectangular shape of the potential at the gate of the source follower but assumes a rectangular input to the switch transistor. In this simulation the input signal is a realistic transition rather than the rectangular impulse on which the timing analysis has been based. Therefore, the 25 ps fall-time annotated on the diagram starts at the end of the input transition which incidentally corresponds to the start of the falling transition at the source follower’s gate terminal.

When the logic gate output is high in the simulation of Fig. 5.3, the source follower’s gate-source junction is forward biased by roughly the built-in potential. When a falling transition occurs at the source follower’s gate the junction is effectively pinched off until the output catches up. Therefore, the gate-source junction voltage change, $\Delta V_{sbf}$, is about two volts and (5-32) gives an optimum $z_{sf}/z_{sw} = 2.04$ for $F = 4$ and an expected fall-time from (5-33) of 49.4 ps which is confirmed by the simulation.
The first feature to note is that the speed is not strongly dependent on the source follower width as any value in the quite wide range \(1.67 < \frac{z_{sf}}{z_{sw}} < 2.8\) gives near maximum transition speed. Therefore, although the analysis (5-19) to (5-34) is based on a simple charging model it is a good design guide and the error in approximation is not significant to the design.

The other feature is this: at the optimum \(\frac{z_{sf}}{z_{sw}}\) ratio, the delay from the top of the input transition to the middle of the source follower's gate transition is equal to the delay between the source follower's gate and the output transition. This is the assumption used to derive the optimum source follower size (5-24) from the total fall-time (5-23). Therefore this assumption is verified by the simulation.

The SPICE simulation shown in Fig 5.4 is of the rising transitions for the same BFL gates used in Fig 5.3. The fastest rising transitions occur in the same range of source follower size as the falling transitions and, again the sensitivity to the source follower size is very weak. The expected rise-time, assuming \(V_{sfl}=V_{sfh}\) from (5-34) is \((24.7+\kappa 37.7)\) ps. Examination of the device model indicates that the reduction in switch transistor capacitance when pinched off is represented by \(\kappa \approx 0.25\). Therefore the expected total rise time is about 34 ps which agrees with the simulation shown in Fig 5.4.
5.3.5 Unbuffered Logic

Unbuffered logic does not include a source follower so the inverting stage is followed directly by the diode level-shift network and, as in Schottky diode FET logic, a fan-out can involve multiple pull-down transistors. In addition to the current of the switch, the pull-up transistor in this type of circuit must also carry the load of the pull-down transistors so the available charging current for a rising output is the pull-down transistor current, \( I_{\text{dss}z_{\text{pd}}} \), less \( fI_{\text{dss}z_{\text{pd}}} \) through \( f \) pull-down transistors and the current through the switching transistor.

\[
I_{\text{available}} = z_{\text{pu}}I_{\text{dss}} - fz_{\text{pd}}I_{\text{dss}} - z_{\text{sw}}(I_{\text{dss}} + g_m V_i) \tag{5-38}
\]
In the unbuffered gate designed for a fan-out \( F \) the pull-up transistor is widened to balance the current through the pull-down transistor. From (5-7)\(^\dagger\):

\[
\frac{z_{pu}}{z_{sw}} = \left(1 - \frac{V_h + V_l}{2V_{po}}\right) z_{sw} + Fz_{pd} \tag{5-39}
\]

The capacitance to be charged is \( Fz_{sw}C_{gs} \), the effective voltage change is \( V_h - V_l \) and the rise-time to 1 neper is independent of relative transistor size:

\[
\tau_r = \frac{1}{1.58} \frac{C \Delta V}{I_{available}}
\]

\[
= \frac{2Fz_{sw}C_{gs}(V_h-V_l)}{1.58z_{sw}g_m(V_h-V_l)} \tag{5-40}
\]

During a falling transition the pull-down transistor is isolated from the inverter stage and other driven gates by the level-shift diodes so the fall-time is determined by the size of a single pull-down transistor.

\[
\tau_f = \frac{1}{1.58} \frac{C \Delta V}{I_{available}}
\]

\[
= \frac{z_{sw}C_{pd}(V_h-V_l)}{1.58g_mz_{pd}(V_h-V_l)} \tag{5-41}
\]

The pull-down transistor can be set so that when \( f = F \) the fall-time equals the rise time. Equating (5-40) and (5-41) gives

\[
\frac{z_{pd}}{z_{sw}} = \frac{V_h-V_l}{2FV_{po}} \tag{5-42}
\]

and then

\[
\tau_f = \tau_r = \frac{1.27FC_{gs}}{g_m} \tag{5-43}
\]

When the fan-out is actually \( f \) the rise-time to 1 neper is found by generalizing (5-40) and using (5-38), (5-39) and (5-42).

\[
\tau_r = \frac{1}{1.58} \frac{C \Delta V}{I_{available}}
\]

using (5-38)

\[
= \frac{2fz_{sw}C_{gs}(V_h-V_l)}{1.58I_{dss}(z_{pu}-fz_{pd}-z_{sw}(1+g_mV_l/I_{dss}))}
\]

using (5-39)

\[
= \frac{1.27FC_{gs}}{g_m\left[1-2\frac{V_{pu}(F-f)z_{pd}}{(V_h-V_l)z_{sw}}\right]}
\]

\( \dagger \quad \frac{z_{pu}}{z_{sw}} = 1 - \frac{V_h - V_l}{2V_{po}} \tag{5-7} \)
This expression increases rapidly as \( f \) approaches \( 2F \) because the loading from the pull-down transistor becomes greater than the available current from the pull-up transistor. The response time rapidly increases as more than \( F \) pull-down elements are added to the output. This deterioration imposes a limitation on the use of unbuffered logic as a standard gate suitable for any fan-out because each gate must be custom designed for the particular load conditions.

\[
\tau_r = \frac{1.27fC_{gs}}{g_m(2F-f)} 
\]  

(5-44)

5.4 A New Logic Family

Buffered logic is far more tolerant of fan-out variations and therefore it is suited to standard cell design approaches. However, the pull-down transistor and source follower occupy a large area. The advantage of unbuffered logic is that it occupies a smaller area and it is faster for small fan-out applications. The ratio of the transition times for buffered and unbuffered topologies (5-33) and (5-43) gives the critical fan-out below which unbuffered logic is faster.

\[
F < \frac{2.31\Delta V_{sh}}{|V_{po}|} 
\]  

(5-45)

The buffered logic topology can be improved by reducing the change in gate-source junction potential, \( \Delta V_{sh} \). A technique for achieving this without affecting the gate operation has been developed and a new logic topology based on this technique called Saturated Buffered FET Logic proposed.

5.4.1 Operation of Saturated Buffered FET Logic

When the gate junction of the source follower in BFL is forward biased a quantity of charge stored in the channel of the device must be removed before a falling transition can occur. This creates additional delay before the output potential can fall (Fig 5.5). The forward bias is not necessary because it does not increase the output potential. This suggests that the gate delay can be reduced, without affecting the gate operation, by limiting the source follower’s gate potential. At the same time the gate-source junction potential change, \( \Delta V_{sh} \), is also reduced. One way to achieve this is by using a separate power supply for the inverter stage to limit its maximum output but this is inconvenient and requires additional wiring.
The basic Saturated Buffer FET Logic (SBFL) inverter circuit is shown in Fig. 5.6. It uses a buffer stage and features the use of a Swing Limiter diode in the inverter stage.

Figure 5.5. Operation of the Buffer stage in BFL.

Figure 5.6. The basic Saturated Buffered FET Logic inverter.

Figure 5.7. Operation of Saturated Buffered FET Logic inverter.

The basic Saturated Buffer FET Logic (SBFL) inverter circuit is shown in Fig. 5.6. It uses a buffer stage and features the use of a Swing Limiter diode in the inverter stage.
The Swing Limiter diode connected in series with the pull-up transistor decreases the potential at the drain of the pull-up transistor and therefore limits the highest potential which can be achieved at the gate terminal of the source follower. This restricts operation of the buffer stage transistors to the saturated mode. The charging and discharging of the gate-source junction of the source follower is greatly reduced (Fig. 5.7). Consequently, SBFL has minimal delay before its output potential falls in response to a rising input.

5.4.2 Advantages of Saturated Buffered FET Logic

The use of the Swing Limiter diode can be extended to any application where a source follower buffer is used. In particular, buffered SCFL can take advantage of the technique as shown in Fig. 5.8. The fan-out at which unbuffered logic is faster, equation (5-45), is proportional to $\Delta V_{th}$ so the use of SBFL can be extended to small load applications. This is an advantage for standard gate cell libraries where it is preferable to use a single topology for both high and low fan-out cells.

The speed of a SBFL ring oscillator can be up to twenty percent faster than BFL and has lower power consumption because time and energy is not expended in charging the gate-source junction of the source follower. There is no reduction in the noise margin. The reduction of logic swing at the drain of the switch transistor is inconsequential because the extra swing served only to charge the source follower's gate junction. The additional wafer area required to accommodate the Swing Limiter diode is typically less than three percent of the total area of the gate.
5.5 Process Variations

The operation of the gate design including operation of dual-gate inputs must be checked at the extremes of process variations. The logic level calculation procedure illustrated in Fig. 5.9 determines the extremes of logic and logic threshold levels for all combinations of variations of the parameters listed in section 4.5.1 (temperature, parasitic resistance, doping level, channel depth, and electrode spacing). The boxes in the diagram represent four identical sets of logic gates driven by the same input level which is the appropriate extreme output from the indicated set.

![Diagram](image)

*Figure 5.9. Flow of logic signals for evaluation of process variation. The boxes represent four identical sets of logic gates driven by the same input level which is the appropriate extreme output from the indicated set.*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{pullup}$</td>
<td>12</td>
</tr>
<tr>
<td>$W_{buffer}$</td>
<td>52</td>
</tr>
<tr>
<td>$W_{switch}$</td>
<td>12</td>
</tr>
<tr>
<td>$W_{nand}$</td>
<td>55</td>
</tr>
<tr>
<td>$W_{pulldown}$</td>
<td>52</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$-2.75$</td>
</tr>
<tr>
<td>$V_{ss}$</td>
<td>$-2.00$</td>
</tr>
</tbody>
</table>

*Figure 5.10. The logic gate design dialogue presented by GaAsSPICE.*

<table>
<thead>
<tr>
<th>Logic Limits</th>
<th>max</th>
<th>nom</th>
<th>min</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic High</td>
<td>0.65</td>
<td>0.35</td>
<td>0.09</td>
</tr>
<tr>
<td>Logic Low</td>
<td>-0.24</td>
<td>-0.44</td>
<td>-0.82</td>
</tr>
</tbody>
</table>

5.5 Process Variations

The operation of the gate design including operation of dual-gate inputs must be checked at the extremes of process variations. The logic level calculation procedure illustrated in Fig. 5.9 determines the extremes of logic and logic threshold levels for all combinations of variations of the parameters listed in section 4.5.1 (temperature, parasitic resistance, doping level, channel depth, and electrode spacing). The boxes in the diagram represent four identical sets of logic gates driven by the same input level. The
extreme of one logic level at the input produces, in the worst case, the extreme of the complementary level. The design is robust against process variation if the worst case logic high is above the highest logic threshold level and the worst case logic low is below the lowest logic threshold level. Note however that the noise margin is reduced when the logic levels are close to the logic threshold level. It is assumed that all the devices in a single logic gate have the same parameters.

Each gate in the set (a box in Fig. 5.9) has piecewise linear MESFET and diode parameters corresponding to one of the combinations of parameter variations. For each gate the input logic level and the piecewise linear models are used in the drain-source potential equations (5-8) to (5-11). Then the output logic levels are given by (5-1) and (5-2). The logic threshold is given by rearranging (5-7)

\[
V_{\text{mid}} = \min \left\{ V_{\text{pu}} \left( \frac{z_{\text{pu}}}{z_{\text{sw}}} - 1 \right), V_{\text{pu}} \left( \frac{z_{\text{pu}}}{z_{\text{sw}}} \frac{I_{\text{dss}}}{I_x} - 1 \right) \right\} \tag{5-46}
\]

To check the operation of dual-gate inputs each set includes gates whose drain-source potentials and logic threshold input levels are calculated for each of the dual-gate device’s inputs. The implementation of this procedure in the GaAsSPICE software (described in Chapter 7) produces a graphical representation of the extreme logic levels and an indication of the various device sizes. The GaAsSPICE design dialogue is shown in Fig 5.10. The designer is able to adjust one or more of the entries and recalculate.

Extensive testing of this algorithm with typical device parameters has indicated that it is sufficient to consider only two extreme sets of parameter variations (apart from the nominal parameters) as listed in Table 5.1. The Low and High Models are the extreme case parameters which include the low and high temperature extremes respectively.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Low Model</th>
<th>High Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T)</td>
<td>Temperature</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>(R_a)</td>
<td>Ohmic Alloy Sheet Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>(R_c)</td>
<td>Ohmic Contact Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>(a)</td>
<td>MESFET channel depth (^\dagger)</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>(N_d)</td>
<td>Nominal doping Level</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>(d_s)</td>
<td>Diode electrode spacing</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>(d)</td>
<td>MESFET electrode spacing:</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td>gate-drain</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>gate-source</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

\(^\dagger\) Initial channel depth extremes are calculated from the pinch-off voltage variation and then the pinch-off variation used is recalculated from the extremes of channel depth and doping.

Table 5.1. Assignment of Process Parameter Extremes.
5.6 Application of Design Procedure

A logic gate design obtained using the results of this chapter forms the basis for building logic cell libraries. The logic gate design procedure produces a template of rules for determining the relative widths of devices in the gate in terms of a desired fan-out and switch transistor size:

- The basic pull-up transistor size, \( z_{pu} / z_{sw} \), given by (5-8)
- The total pull-up transistor size, \( z_{pu\text{ total}} \), given by (5-12)
- The dual-gate switch transistor size, \( z_{an} / z_{pu} \), given by (5-15)
- The diode chain size, \( z_d / (z_{pd} = z_{sd}) \), given by (5-17) and (5-18)
- The source follower size, \( z_{sf} / z_{sw} \), given by (5-32)

A logic gate library can be generated automatically from this template. A family of gates is created by different combinations of dual- and single-gate switches. The family’s power and fan-out is set by scaling the switch transistor and altering the relative size of the buffer and logic stages in accordance with (5-32). The buffer stage is a single scaleable entity so that its size can be adjusted to suit the fan-out requirements. A pull-up transistor is also available as a discrete element for combining with single and dual gate switches. Thus there are four scaleable elements which can be put together to create a gate family. The listing in section 5.6.1 shows these elements as subcircuits BUF, JPU, NOR and AND.

The automation of the gate design procedure and library generation with the template as described above forms the core of a software package, \textit{GaAsSPICE}, described in Chapter 7. This package was developed because frequent changes to the fabrication process made it necessary many times between fabrication runs to recreate completely the logic library.

5.6.1 Example

The following listing is included here as an example of a logic gate family and will be referenced in Chapter 6. A separate file (not shown) is used to list the standard cells such as inverters, two input NAND gates, NAND/NOR gates and basic flip-flops and registers. The cells are duplicated in the various power ratings. Each cell is a subcircuit composed of the device subcircuits from the model definition listing given below. The task of updating the entire library is accomplished by updating this model listing.
This SPICE deck is designed for version 3b1 or later. It provides a set of reference model cards for GaAs BFL gate elements which can be used for extracting the simplified linear properties of the elements.

**.MODEL Cards**

These are MESFET, Diode, and capacitance models for 1 micron wide devices.

```
.MODEL MESFET NJF Vto=-1.5 Beta=280u Xi=0.15 Eta=41m Lambda=45m Rs=1733
  Rd=1733 Cgs=1.6f Cgd=0.18f Pb=0.702 IS=3040f Kappa=0.2 Theta=5 cm=2

The upper gate of a dual gate FET has zero source resistance

.MODEL MESand NJF Vto=-1.5 Beta=280u Xi=0.15 Eta=41m Lambda=45m
  Rd=1733 Cgs=1.6f Cgd=0.18f Pb=0.702 IS=3040f Kappa=0.2 Theta=5 cm=2

Parasitic capacitances between FET electrodes

.MODEL Cds C C J=0.067FF CJ=0.087FF DEF=1
.MODEL Cgs C C J=0.087FF DEF=1
.MODEL Cgd C C J=0.067FF DEF=1

* capacitance between gates of a dual gate FET

.MODEL Cgg C C J=0.067FF DEF=1

.MODEL Schottky D IS=7599f Rs=1733 N=1.09 CJ=0f VJ=0.7 EG=0.71 Xti=2.18 BV=9.4
* Diode Parasitic capacitance

.MODEL CD C C J=0.1134FF CJ=0 DEF=1
```

**Power Supplies**

```
Vvdd vdd 0 3.50V
Vvss vss 0 -3V
```

**Medium Speed BFL Transistors**

```
.SUBCKT NOR Drain Gate
jMESFET Drain Gate 0 MESFET 18
Cds Drain 0 Cds L=18
Cgs Gate 0 Cgs L=18
Cgd Drain Gate Cgd L=18
.ENDS NOR

.SUBCKT JPU Vdd Source
jMESFET Vdd Source Source MESFET 7
Cds Vdd Source Cds L=7
*Cgs Source Source Cgs L=7
Cgd Vdd Source Cgd L=7
rleak Vdd Source leak 1meg
.ENDS JPU

.SUBCKT AND Drain Fast Slow
jUpper Drain Fast x MESand 24
jLower Drain x Slow 0 MESFET 24
Cds Drain 0 Cds L=24
Cdd Drain Fast Cgd L=24
Css Slow 0 Cgs L=24
Cgg Fast Slow Cgg L=24
rLeakL x 0 1meg
rLeakU Drain x 1meg
.ENDS AND
```
The SPICE listing includes models for one micron wide MESFET devices and parasitic interelectrode capacitances. It continues with the definition of a 24 μm dual-gate FET, a pull-up transistor and a buffer stage for the gate shown in Fig. 5.2. This set of gate elements is duplicated to give a half power family simply by halving the device widths. The MESFET characteristics shown in Fig. 5.1 were produced by this SPICE model definition which was created with the procedure described in Chapter 4.
5.7 Summary

This chapter has developed a logic gate design procedure which accommodates process variations and can be automated.

A simple linear transistor model is used to select the relative sizes of the transistor elements in a logic gate to give minimum switching time for a particular load. The inverter pull-up transistor is chosen relative to the switching transistor so that the input logic threshold is midway between the high and low logic levels. The source follower and pull-down transistors are chosen so that the gate delay is a minimum for the designed fan-out. It is also confirmed that the transit time under the MESFET gate is a suitable figure of merit for the fabrication process.

The gate design including operation of dual-gate inputs is checked at the extremes of process variations. Then it is used as a template for the automatic generation of a standard logic cell library which simplifies the design of complex digital circuits.

A new logic family called Saturated Buffered FET logic (SBFL) which achieves the fan-out performance and speed of buffered logic with reduced power and circuit area is proposed. In SBFL, the use of a Swing Limiter diode in conjunction with the pull-up transistor gives a speed improvement of up to twenty percent and a reduction in power consumption.

The next chapter explores an efficient circuit simulation technique and extends the automation of cell library generation to the generation of equivalent circuit models.

5.7.1 Chapter 5 Reference

6 Extraction of a Switched-Linear Network Model

6.1 Introduction

A switching circuit, such as a Buffered FET Logic (BFL) gate, can be accurately simulated using a discrete SPICE element for each component. When large circuits are being simulated this can require a large computational effort and it is essential to have a much simpler, and therefore quicker, model. In order to reduce the computational burden for large circuits, switch-level models, which consider transitions as scheduled events, are commonly used. The RC timing models used in switch-level simulators [Chawla et al. 1975, Bryant 1981, Terman 1983, Pfister 1986, Chu and Horowitz 1988] are satisfactory for many purposes. However, such models require a considerable effort in circuit characterisation over a range of load conditions to yield, at best, a set of conservative delays which ensure that predicted circuit speeds will be achieved. In practice the finer details of signal transition times and glitch behaviour are often neglected or given inadequate attention in the pursuit of simplicity. In high performance Gallium Arsenide technology, circuits are pushed to their limit and design margins can be small, so more detailed models which allow exploration of circuit behaviour beyond conservative limits are required.

The switched-linear network gate modelling technique presented here overcomes these limitations. It is computationally efficient, allowing simulation of large circuits, and gives an accuracy comparable to that obtained with device-level SPICE models. In
addition, the model has a structural basis which inherently accounts for gate loading and permits accurate automatic extraction from a device-level SPICE simulation.

The next section describes the principle of switched-linear networks and the general procedure for developing the models. Then section 6.3 describes the basic procedure used to determine the operating regions of transistors in the circuit being modelled and how a linear network is fitted to the region. Section 6.4 demonstrates this procedure by modelling each device in a BFL logic gate by describing the operation of the device and its switched-linear network and then by describing the regions to which the networks are fitted. These device models are then assembled to produce a switched-linear network model for the gate. Finally, the gate model’s performance is demonstrated in section 6.5 with the simulation of a serial multiplier.

6.2 Switched-Linear Network Models

Each section of a logic gate consists of active components between an input node and an output node. The input node presents a loading capacitance to the device driving it and the output node presents a linear network comprising a current source, a conductance and a capacitance to the device it drives. Simulating this is simplified by assuming that each node in the circuit is affected by a simple switching action of the linear network presented by each driver. Simulator convergence and speed are improved by disallowing the use of node-to-node components. However, accuracy is maintained by switching between a number of linear networks which each model a different region of gate operation depending on the potentials of the driven and input nodes. A careful analysis of gate operation can be used to determine the minimum number of relevant gate operating regions. For example, it is not necessary to model regions of a device in which it does not operate. Indeed, a best fit model of the whole operating region compromises the accuracy in some regions and if the device operates only in these regions the model would be totally inaccurate.

The exact structure of a switching model is found by considering each element in the logic gate and its influence on the external nodes of the gate. A complete SPICE [Quarles 1989] simulation serves as a reference. Each device’s SPICE model is substituted, one at a time, by a switched-linear network model based on a hypothesis of how it influences the circuit. Each effect is then investigated by adding or removing it from the model to confirm that it is as hypothesized. For the purposes of this testing procedure, the model is built up using SPICE3 linear circuit elements and switches.
This method isolates and highlights the critical components and their effects on the circuit giving clear insight into its operation.

6.3 Extraction of Switched Network Models

A rudimentary switched-linear network model of a transistor is a set of linear functions which follow the basic characteristics of the device. Referring to Fig. 6.1, in the saturated mode, the drain conductance is constant and the current is proportional to the gate bias. In the linear mode, the drain conductance is higher and its modelled value is selected to cover adequately the range of operation for each device depending on its function.

The operating range and condition of each device are determined using several test circuits. These include logic gates operating in various states: one with a high output, one with a low output and one with a logic threshold level. In a SPICE simulation, two gates can be wired in a ring so that a high and low level will be at each input. Another gate with its input connected to its output will have an input level at the logic threshold. The devices in these gates operate in one of the three states which are identified as **High, Mid and Low** depending on the output of the gate in question (these states
are labelled H, M, and L respectively in the figures which follow). Additional operating states can be simulated by using transistors biased by controlled sources set to match the conditions in the three test gates. The different operating modes are then probed in situ to find the best linear model. Additional data on the ac characteristics are derived directly from the model cards.

The parallel conductance and current source which passes through operating states \((I_1, V_1)\) and \((I_2, V_2)\) is given by:

\[
G = \frac{I_1 - I_2}{V_1 - V_2} \quad (6-1a)
\]

\[
I = -I_1 + V_1 G \quad (6-1a)
\]

The process of measuring the test circuits and determining the linear models is easily automated using the programming language included with SPICE3. Automation also guarantees the accuracy of the model parameters.

### 6.4 Switched Network for BFL Gates

The BFL gate serves as an example for demonstrating the development of a switched-linear network model. As described in Chapter 2, the gate includes a logic stage with a pull-up transistor and switch transistors. There is also a buffer stage with source follower, pull-down transistor and the diode level shifter required by depletion mode MESFET devices (Fig. 6.2).
6.4.1 Switched Models of Buffer Stage Components

The Pull-down Transistor

The pull-down transistor is normally operated in the saturated mode as a constant current source for the buffer stage. An accurate model of this transistor is a current source, $I_{PD}$, in parallel with a conductance, $G_{PD}$. It must be noted that when the logic gate output is low, it may operate in the knee region between the saturated and linear modes. Since entering this mode is a significant factor in determining the output low logic level, its model must have two states depending on the relation of drain potential to a critical knee voltage, $V_{kpd}$, as shown in Fig. 6.3.

The parasitic drain resistance of the device is negligible, being only a few ohms compared with thousands of ohms for the device resistance, so the equivalent parallel capacitance, $C_{PD}$, is the sum of the parasitic interelectrode and the gate-drain junction capacitances as determined from the model parameters.
The dc model is defined by four parameters in (6-2) which are extracted from a SPICE simulation.

\[
I_{PD} = \begin{cases} 
-I_{dspd} & \text{when } V_{OUT} > V_{kpd} \\
V_{kpd}(G_{kpd} - G_{spd}) - I_{dspd} & \text{when } V_{OUT} \leq V_{kpd}
\end{cases} \tag{6-2a}
\]

\[
G_{PD} = \begin{cases} 
G_{spd} & \text{when } V_{OUT} > V_{kpd} \\
G_{kpd} & \text{when } V_{OUT} \leq V_{kpd}
\end{cases} \tag{6-2b}
\]

\[
C_{PD} = C_{ds\text{ }Parasitic} + C_{gd\text{ }Junction} + C_{gd\text{ }Parasitic} \tag{6-2c}
\]

The first two parameters are the saturated mode conductance, \(G_{spd}\), and current, \(I_{dspd}\), which are set to fit the \textit{Mid} and \textit{High} operating states. The other two parameters, \(G_{kpd}\) and \(V_{kpd}\), define the knee region and are set to fit the \textit{Low} state and another operating state with current just below saturation.

\[
I_{pd\text{ }knee} = \frac{1}{2} I_{pd\text{ }low} + \frac{1}{2} (2I_{pd\text{ }mid} - I_{pd\text{ }high}) \tag{6-3}
\]

This current is set to the average of the \textit{Low} state current and the current extrapolated from the \textit{Mid} and \textit{High} state currents. This test state is generated by a subcircuit with a pull-down transistor and a controlled current source set to a current determined from the currents in the three test gates.

The capacitance model parameters cannot be determined from the test circuits and are passed directly from the model parameters.

\textit{Diode Chain}

The simplest component in the BFL gate is the diode chain which can be described by a standard textbook model – a series resistance, \(R_D\), and voltage, \(V_D\), with a parallel capacitance, \(C_D\) (Fig. 6.4). The effective parallel capacitance is made up of the parasitic capacitance between the diode’s external terminals and junction capacitance, \(C_{jo}\), which is isolated from the diode’s external terminals by a parasitic series resistance, \(R_s\).
These components can be calculated from the model parameters for η diodes assuming that current through them is \((I_{PD} + V_{OUT\text{ mid}/G_{PD}})\):

\[
R_D = \eta \left\{ R_s + \frac{NkT}{q(I_{PD} + V_{OUT\text{ mid}/G_{PD}})} \right\} \quad (6-4a)
\]

\[
V_D = \eta \frac{NkT}{q} ln\left(\frac{I_{PD} + V_{OUT\text{ mid}/G_{PD}}}{I_s}\right) \quad (6-4b)
\]

\[
C_D = \frac{1}{\eta} C_{\text{Parasitic}} + C_o\left(1 - \frac{\eta R_s}{R_D}\right) \quad (6-4c)
\]

The model elements are better calculated from the standard SPICE simulation test states. The resistance is the ratio of the differences between each diode chain’s voltage drop and current in the High and Low states. Having determined the resistance, the equivalent potential is set to pass through the Mid state. This procedure is adequate because the voltage drop over the diode chain is responsible for the critical level shift in the region of the Mid state. Near the High and Low states the level shift caused by the diode chain is not critical because it is hindered by the saturation effects of other devices in the gate.

**Source Follower Transistor**

The source follower model is developed with the aid of Fig. 6.5.

The source follower is modelled by a series voltage and resistance. In this case the voltage source contains both a dc component, \(V_{SF}\), which includes the power supply and a component proportional to the gate-source potential with gain, \(A_{SF}\). The source follower operates in both the saturated and linear modes. In the saturated mode the buffer stage operates at unity gain and the source follower’s gate-source bias is near
zero. The gain is the product of the transconductance, $G_m$, and the saturated mode drain-source resistance, $R_{ds}$.

In the linear mode, when the source potential, $V_{ssf}$, exceeds the knee voltage, $V_{ksf}$, the source follower’s gate-source bias increases dramatically so that it can deliver the required current to the pull-down transistor. Here, the drain-source potential is proportional to the gate-source potential with gain, $A_{sflin}$, so the drain-source resistance is selected for correct proportionality rather than to follow the transistor characteristic (i.e. the modelled linear mode I-V characteristics do not converge to the origin in Fig. 6.5). The equivalent capacitances between gate-drain and drain-source are the sum of the parasitic interelectrode and the gate-drain junction capacitances.

\[
V_{SF} = \begin{cases} 
V_{sfo} & \text{when } V_{ssf} < V_{ksf} \\
V_{ksf} - \frac{A_{sflin}}{G_m R_{ds}}(V_{ksf} - V_{sfo}) & \text{when } V_{ssf} \geq V_{ksf}
\end{cases}
\]  

(6-5a)

\[
A_{SF} = \begin{cases} 
G_m R_{ds} & \text{when } V_{ssf} < V_{ksf} \\
A_{sflin} & \text{when } V_{ssf} \geq V_{ksf}
\end{cases}
\]  

(6-5b)

\[
R_{SF} = \begin{cases} 
R_{ds} & \text{when } V_{ssf} < V_{ksf} \\
A_{sflin} \frac{1}{G_m} & \text{when } V_{ssf} \geq V_{ksf}
\end{cases}
\]  

(6-5c)

\[
C_{dsf} = C_{ds \text{ Parasitic}}
\]  

(6-5d)

\[
C_{gdsf} = C_{gd \text{ Junction}} + C_{gd \text{ Parasitic}}
\]  

(6-5e)

In addition to the test gates another set of subcircuits with source follower transistors is used to fit the linear model parameters. The bias voltages from the test transistors are found from the test gates.

The saturated mode clearly exists between the Mid and Low operating states and the linear network model for this mode is fitted to these states. Three parameters are required. The first two are the dc voltage drop at zero input, $V_{sfo}$, and the drain-source resistance, $R_{ds}$. These are determined for a constant input potential using two source followers with zero gate-source potential each with a drain-source potential equal to that of the Mid and Low states respectively. The third parameter is the transconductance, $G_m$, which is determined at the Mid state drain-source potential using another two source followers with Low and High state gate-source potentials respectively.
The linear mode gain, $A_{\text{slin}}$, and equivalent knee voltage, $V_{\text{ksf}}$, are found with the High state circuit and another source follower operating with a drain-source potential at the knee state given by:

$$V_{ds} = 0.1V_{dshigh} + 0.9(2V_{dsmid} - V_{dslow}) \quad (6-6)$$

This drain-source potential is a weighted average of the measured high state potential and a high state potential extrapolated from the mid and low states assuming that the voltage swing from High to Mid is the same as from Mid to Low. The weighting was chosen by experiment to produce a knee state which gives the most accurate model.

### 6.4.2 Assembled Buffer Stage

The buffer stage is assembled to form a single switched node, $V_{\text{OUT}}$, controlled by an input node, $V_{\text{IN}}$, (Fig. 6.6a). The component values at these nodes are dependent on the internal node potential at the source terminal of the source follower, $V_{\text{ssf}}$, and it is necessary to express this in terms of the external potentials. Expression (6-7) is derived for a given output potential, $V_{\text{OUT}}$. The potential across $R_D$ of the diode’s switched-linear
model is $V_{\text{OUT}} - V_D - V_{\text{ssf}}$. The current through $R_D$ also flows through the source follower and $V_{\text{ssf}}$ is the total voltage drop across the source follower’s switched-linear model:

$$V_{\text{ssf}} = R_{\text{SF}} \frac{V_{\text{OUT}} - V_D - V_{\text{ssf}}}{R_D} + \{ V_{\text{SF}} + A_{\text{SF}} (V_{\text{IN}} - V_{\text{ssf}}) \}$$

which yields

$$V_{\text{ssf}} = \frac{R_{\text{SF}}}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} V_{\text{OUT}} + \frac{R_D V_{\text{SF}} - V_D R_{\text{SF}}}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} + \frac{R_D A_{\text{SF}}}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} V_{\text{IN}} \quad (6-7)$$

The equivalent output node current is the current through $R_D$ when $V_{\text{OUT}} = 0$ summed with the contribution from the pull-down transistor:

$$I_{\text{BF}} = \frac{V_D + V_{\text{ssf}}}{R_D} + I_{\text{PD}} = \frac{V_{\text{SF}} + V_D (1 + A_{\text{SF}})}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} + \frac{A_{\text{SF}} V_{\text{IN}}}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} + I_{\text{PD}} \quad (6-8a)$$

The output node conductance is given by

$$G_{\text{BF}} = \frac{1 + A_{\text{SF}}}{R_{\text{SF}} + R_D (1 + A_{\text{SF}})} + G_{\text{PD}} \quad (6-8b)$$

The component values in (6-8) are determined by (6-2), (6-4), (6-5) and (6-7). This may look complicated but it is simply a three region piece-wise linear function of the input and output potentials.

The capacitance at the output is the sum of the contributions from each device.

$$C_{\text{BF}} \text{ OUT} = C_{\text{dsf}} (1 + R_D G_{\text{spd}}) + C_{\text{PD}} + C_D R_D G_{\text{spd}} \quad (6-9)$$

The capacitance at the input is dominated by the equivalent Miller-effect capacitance of the source follower’s gate-source junction. This capacitance must take on several values in order to model the behaviour of the buffer over an entire high-low-high cycle. The buffer stage gain, $A_{\text{buf}}$, and the junction capacitance vary during this cycle. It is also important to include the effect of the source follower’s parasitic source resistance, $R_{\text{ssf}}$, which reduces the effective junction capacitance in the linear region, $V_{\text{ssf}} > V_{\text{ksf}}$, where the output is at a high potential and the gate-source junction is forward biased. When the output is lower, the parasitic resistance is not significant and the simple sum of the parasitic and junction capacitances is used.
\[ C_{\text{BF IN}} = (1-A_{\text{buf}}) C_{\text{gsaf}} + C_{\text{gsaf Junction}} + C_{\text{gsaf Parasitic}} \]  

(6-10a)

When \( V_{\text{gsf}} > V_{\text{kaf}} \)

\[ C_{\text{gsaf}} = C_{\text{gsaf Junction}} \left( 1 - \frac{R_{\text{gsaf}}}{R_{\text{desf}}} \right) + C_{\text{gsaf Parasitic}} \]  

(6-10b)

\[ A_{\text{buf}} = \frac{G_m R_{\text{dsd}} (R_{\text{PD}} + R_{\text{D}})}{(1+G_m R_{\text{dsd}})(R_{\text{PD}} + R_{\text{D}}) + R_{\text{SF}}} \]  

(6-10c)

or else when \( V_{\text{OUT}} > V_c \)

\[ C_{\text{gsaf}} = \frac{1}{2} \frac{C_{\text{gsaf Junction}}}{1 - \frac{R_{\text{gsaf}}}{R_{\text{desf}}}} + C_{\text{gsaf Parasitic}} \]  

(6-10d)

\[ A_{\text{buf}} = \frac{G_m R_{\text{dsd}} (R_{\text{PD}} + R_{\text{D}})}{(1+G_m R_{\text{dsd}})(R_{\text{PD}} + R_{\text{D}}) + R_{\text{SF}}} \]  

(6-10e)

or else when \( V_{\text{OUT}} < V_{\text{IN}} \times \frac{A_{\text{affin}}}{(1+A_{\text{SF}}) + R_{\text{SF}} G_{\text{kpd}}} + V_{\text{OUT}}(V_{\text{IN}}=0) \)

\[ C_{\text{gsaf}} = C_{\text{gsaf Junction}} + C_{\text{gsaf Parasitic}} \]  

(6-10f)

\[ A_{\text{buf}} = \frac{A_{\text{affin}}}{(1+A_{\text{SF}}) + R_{\text{SF}} G_{\text{kpd}}} \]  

(6-10g)

Otherwise

\[ C_{\text{gsaf}} = C_{\text{gsaf Junction}} + C_{\text{gsaf Parasitic}} \]  

(6-10h)

\[ A_{\text{buf}} = \frac{A_{\text{affin}}(R_{\text{PD}} + R_{\text{D}})}{(1+A_{\text{affin}})(R_{\text{PD}} + R_{\text{D}}) + R_{\text{SF}}} \]  

(6-10i)

The dc transfer characteristic displays a constant level shift with unity gain in the main region of operation. At either extreme, there is a saturation effect as either the pull-down or source follower move into the linear mode of operation as shown in Fig. 6.6b.

The transient operation is complicated by the variable Miller-effect capacitance of the source follower. At the start of a rising edge, the effective input capacitance is moderate while the pull-down is in the linear mode and the Miller effect is significant because the buffer stage has less than unity gain (i.e. zero Miller effect). During the output rising transition the input capacitance is small because the buffer has near unity gain. At the top of the rising edge the capacitance rises as the source follower’s gate junction runs into forward bias condition and the gain of the buffer reduces. This region is passed momentarily and does not have a substantial influence.
During the initial part of a falling transition the gain is low because the output response lags the input so the Miller-effect capacitance is large. As the input falls a region of moderate gain is passed where the Miller effect is also moderate. The capacitance then reduces to a low value in the region of unity gain before finally reverting to a moderate value as the gain of the buffer reduces because the pull-down transistor saturates.

The model takes into account the effect of output loading on input capacitance by including a dependency on the output potential. This dependency must be chosen to correctly model the effect of output loading. Heavy gate loading or fast input transitions have the effect of increasing the output verses input hysteresis loop as shown in Figs. 6.6c and 6.6d. The shaded areas in Fig. 6.6 show the unity gain regions selected so that the correct Miller-effect capacitance is applied as the gate loading changes.

A characteristic of BFL is the delayed response of the buffer stage to a falling input. This occurs because the gate-source junction of the source follower is forward biased and channel charge must be removed before it can follow the input. This is modelled in the switched-linear network by the large Miller-effect input capacitance when

\[ C_{V_{in}} \]

\[ V_{in} \]

\[ V_{out} \]

\[ C_{bf} \]

\[ I_{bf} \]

\[ C_{bf} \]

\[ C_{in} \]

\[ V_{in} \]

\[ V_{out} \]

\[ C_{id} \]

\[ V_{in} \]

\[ V_{out} \]

\[ C_{id} \]

\[ V_{in} \]

\[ V_{out} \]

\[ C_{id} \]

\[ V_{in} \]

\[ V_{out} \]

\[ C_{id} \]

\[ V_{in} \]
the source follower is in the linear mode. The new SBFL family described in section 5.4 of Chapter 5 enhances speed by not driving the source follower into linear mode.

In summary, the Buffer Stage model is made up of four components; two capacitances, a current source and a conductance. These components take on different values depending on the input and output potentials. The dc model for the buffer stage is a three region model. The output capacitance is constant and the input capacitance is a five region model.

6.4.3 Inverter Stage Elements

The switching stage components are treated in the same way as the buffer stage to produce switched-linear network representations for the pull-up transistor, the single gate switches and the dual gate switches. These are combined to form NAND/NOR logic elements.

**Pull-up Transistor**

In a manner similar to the pull-down transistor, the pull-up operates in both the saturated and linear modes. The main difference in the dc model is that the entire linear region is modelled rather than just the knee region (Fig. 6.7).

\[
I_{PU} = \begin{cases} 
-I_{dspu} & \text{when } V_{pu} \leq V_{kpu} \\
V_{kpu}(G_{lpu} - G_{spu}) - I_{dspu} & \text{when } V_{pu} > V_{kpu}
\end{cases}
\]

\[
G_{PU} = \begin{cases} 
G_{spu} & \text{when } V_{pu} \leq V_{kpu} \\
G_{lpu} & \text{when } V_{pu} > V_{kpu}
\end{cases}
\]

\[
C_{PU} = C_{ds\ Parasitic} + C_{gd\ Parasitic} + C_{gd\ Junction}
\]
The dc model is defined by four parameters in (6-11). Two of these are the saturated mode conductance, $G_{spu}$, and current, $I_{dspu}$, which are set to fit the Mid and Low operating states. The other two parameters, $G_{lpd}$ and $V_{kpd}$, define the linear region and are set to fit the High state and another operating state with current, $I_{putest}$, below saturation.

$$I_{putest} = 0.25I_{puhigh} + 0.75(2I_{pumid} - I_{pulow})$$  \hspace{1cm} (6-12)

This current was chosen by experiment as a weighted average of the High state current and a high state current extrapolated from the Mid and Low states assuming that the current swing from High to Mid is the same as Mid to Low.

The NOR Switch Transistor

The switch transistor is modelled by a conductance, $G_{SW}$, and a current source, $I_{SW}$, with a transconductance from gate to drain. Near the typical dc operating point the transistor has a relatively low transconductance, $g_{ml}$. However, to simulate properly the charging characteristics of the device when the gate potential is high (greater than a parameter voltage, $V_p$) it is necessary to have a higher transconductance, $g_{mh}$ so that the correct high drain current is produced when the gate potential is suddenly raised. The model achieves this with a two piece description of transconductance (Fig. 6.8).

$$I_{SW} = \begin{cases} 
0 & \text{when } V_{gs} \leq V_{po} \\
I_{dsw} + g_m V_{gs} & \text{when } V_{pu} \geq V_{ksw} \\
V_{kw} \left( g_m/A_{swlin} - G_{sw} \right) - I_{dsw} - g_m V_{gs} & \text{when } V_{pu} < V_{ksw} \end{cases}$$  \hspace{1cm} (6-13a)

$$g_m = \begin{cases} 
g_{mh} & \text{when } V_{gs} > V_p \\
g_{ml} & \text{when } V_{gs} \leq V_p \end{cases}$$  \hspace{1cm} (6-13b)

$$G_{SW} = \begin{cases} 
\infty & \text{when } V_{pu} > \frac{1}{2} (V_{dd} - V_{kpu}) \\
G_{sw} & \text{when } V_{pu} \geq V_{ksw} \text{ and } V_{pu} \leq \frac{1}{2} (V_{dd} - V_{kpu}) \\
g_m/A_{swlin} & \text{when } V_{pu} < V_{ksw} \end{cases}$$  \hspace{1cm} (6-13c)

The drain-source conductance has two values defined for the linear and saturated modes and becomes very large in a near-pinchoff mode. The switch transistor drain potential is above the pull-up knee when it is pinched off so this criterion is used to define the near-pinchoff mode. Note that the drain potential of the switch transistor is $V_{pu}$.

The effective input capacitance is a function of the input and output potentials. When the switch is pinched off there is a low capacitance made up of the gate-drain and the gate-source capacitances. In this case the gate-source junction capacitance has a value similar to the gate-drain junction capacitance. When the switch is not pinched off
the gate-source junction capacitance increases. There is also a large Miller-effect capacitance, \( C_m \), which is significant during the high gain region of an output transition, when \( \alpha V_{ksw} \leq V_{pu} \leq V_{kpu} \). This capacitance is calculated from the gain of the switch/pull-up combination and the coefficient \( \alpha = 2.75 \) was chosen by experiment to set the correct high gain region.

\[
C_{SW\ IN} = \begin{cases} 
  C_m + C_{gs\ Fringe} + C_{gs\ Parasitic} & \text{when } V_{sw\ in} \leq V_{po} \\
  C_m + C_{gs\ Junction} + C_{gs\ Parasitic} & \text{when } V_{sw\ in} > V_{po} 
\end{cases} 
\]

\[
C_m = \begin{cases} 
  1 + \frac{g_{ml}}{G_{SW} + G_{PU}} (C_{gd\ Junction} + C_{gd\ Parasitic}) & \text{when } \alpha V_{ksw} \leq V_{pu} \leq V_{kpu} \\
  C_{gd\ Junction} + C_{gd\ Parasitic} & \text{otherwise} 
\end{cases} 
\]

A delay normally occurs before the output rises because it is slightly lowered by the falling current input through gate-drain capacitance. Since node-to-node elements are avoided in the switched network model, the gate-drain capacitance is added to the output drain-source capacitance to delay the signal by slowing the initial rise of the output. Simulations showed that when \( V_{pu} \) is less than \( \alpha V_{ksw} \) the reverse direction (output to input) gain of the switch/pull-up combination is not zero and produces a significant Miller-effect capacitance change at the output:

When \( V_{pu} < \alpha V_{ksw} \)

\[
C_{SW\ OUT} = C_{ds\ Parasitic} + (C_{gd\ Junction} + C_{gd\ Parasitic}) \left( 1 + \frac{G_{SW} + G_{PU}}{g_{ml}} \right) 
\]

Otherwise

\[
C_{SW\ OUT} = C_{ds\ Parasitic} + (C_{gd\ Junction} + C_{gd\ Parasitic}) 
\]

This drain-source capacitance is critical to correct timing which suggests that the drain node should be the subject of careful circuit layout for maximum speed.

The switch transistor operates in the saturated mode when the gate is in the \textit{Mid} state. The equivalent drain-source conductance, \( G_{ssw} \), and current, \( I_{ds\ ss} \), are set to fit this state and another state generated by a switch transistor with the \textit{High} state drain-source potential but with the same input that produces the \textit{Mid} state. This effectively
fits the drain-source conductance and current independently of gate-source potential.

The transconductance in the high input potential region, \( g_{mh} \), is selected to fit the \textit{Mid} state and another state generated by a switch transistor with the \textit{Mid} state drain-source potential but with the gate potential that produces the \textit{Low} state. This fitting is at constant drain-source potential.

When a high input potential is applied (\textit{Low} state) the switch operates in the linear mode. The voltage gain in this mode, \( A_{\text{swlin}} \), is found from the \textit{Low} state and another switch/pull-up combination with an input half-way between the \textit{Low} and \textit{Mid} state inputs.

The effective pinch-off potential, \( V_{po} \), and low input transconductance, \( g_{ml} \), are measured with two switch transistors with a \textit{High} state drain potential. The gate potential is arbitrarily set to the \textit{Mid} state potential and each source is fed with a controlled current source to generate two operating states with currents

\[
I_{\text{swtest1}} = 0.9 I_{\text{swhigh}} + 0.1 I_{\text{swlow}} \quad \text{(6-16a)}
\]

\[
I_{\text{swtest2}} = 0.5 I_{\text{swhigh}} + 0.5 I_{\text{swlow}}. \quad \text{(6-16b)}
\]

The parameter \( V_p \) is selected as the intersection of the high and low transconductance regions.

\textbf{The NAND Switch Transistor}

The NAND Switch is a dual gate FET which is considered as two FET’s in series; an upper gate at the drain end and a lower gate at the source end. The lower FET is effectively a controlled source resistance for the upper FET and reduces its effective transconductance by a factor \( K \). The drain current is the minimum that the two FET’s will each allow. The dual gate FET is modelled by a single gate FET controlled by the minimum of the drain-end gate potential and the scaled source-end gate potential.

\[
V_{\text{IN SW}} - V_{po} = \min(V_{\text{IN upper}} - V_{po}, K \times (V_{\text{IN lower}} - V_{po})) \quad \text{(6-17)}
\]

The effective pinch-off voltage, \( V_{po} \), is the same as that of the single gate NOR transistor.

The upper gate’s input capacitance is the same as the single gate NOR transistor model except that the Miller-effect capacitance is added only if the lower input is higher than the upper, otherwise the device has little gain.
The lower gate's input capacitance is also the same as the single gate NOR transistor model except that the Miller component, $C_m$, is not present because it is isolated by the upper gate.

\[
C_{\text{LOWER IN}} = \begin{cases} 
C_{\text{gd Junction}} + C_{\text{gd Parasic}} + C_{\text{gs Fringe}} + C_{\text{gs Parasic}} & \text{when } V_{\text{lower in}} \leq V_{po} \\
C_{\text{gd Junction}} + C_{\text{gd Parasic}} + C_{\text{gs Junction}} + C_{\text{gs Parasic}} & \text{when } V_{\text{lower in}} > V_{po}
\end{cases}
\]

In addition, when the lower gate causes an output transition, it must also charge the upper gate junction. This loading is equivalent to an extra capacitance, $C_{\text{slow}}$, added to the logic stage output capacitance during the rising or falling part of a transition. It is necessary to add this component only during a switching transition of the low input otherwise it will be incorrectly added in complex gates even when the dual gate device is not switching.

\[
C_{\text{slow}} = \begin{cases} 
C_{\text{gs Parasic}} + C_{\text{gs Fringe}} & \text{when } V_{\text{in upper}} - V_{pu} \leq V_{po} \text{ & } V_{\text{in upper}} > V_{\text{in lower}} > V_{po} \\
C_{\text{gs Parasic}} + C_{\text{gs Junction}} & \text{when } V_{\text{in upper}} - V_{pu} > V_{po} \text{ & } V_{\text{in upper}} > V_{\text{in lower}} > V_{po} \\
0 & \text{otherwise}
\end{cases}
\]

The necessity of this capacitance clearly identifies the reason why the lower gate is the slower input of a NAND gate. Simulation has confirmed that the loading, $C_{\text{slow}}$, which models the slowing of the lower gate must be at the output and not at the lower input. Thus the effect is inherent in the NAND structure and techniques such as increasing the drive to the slow input will not necessarily decrease its response time.

The output capacitance is the same as the single gate NOR transistor's, (6-14), with the addition of $C_{\text{slow}}$ during switch transitions.

The model parameters are extracted from the dual gate transistor wired as a single gate device. The lower gate is turned on by setting its gate to the logical high potential. Then the upper gate is treated as a single gate transistor and the same procedure used with the single gate NOR transistor is applied to produce a switched-linear network model. This becomes the single gate model controlled by $V_{\text{SW IN}}$ in (6-17).

The parameter $K$ in (6-17) is set so that drain current predicted by the switched-linear network model is the same as a test device. This condition is measured with both their upper gates turned on by a logical high input and with a Mid state input potential is at their lower gates.
6.5 Example

In order to demonstrate the performance of switched-linear network modelling, a circuit design and simulation were carried out using a standard BFL gate library. The library is the SPICE listing of the one micron device model including the parasitic inter-electrode capacitances and the gate template developed as an example in Chapter 5. From the gate template two families of basic logic gates were generated with 12 and 24 micron switch transistors and designed for a fan-out of 4. As mentioned in section 6.3, the extraction of the switched network model has been automated with SPICE3. This produces raw data which is entered to a formatting routine to produce the switched network model listing. For the purposes of testing the procedure, the model is built up using SPICE circuit elements and switches. A corresponding switch-linear network model was generated for each gate in the full device-level SPICE library.

A simple circuit has been demonstrated [Parker and Skellern 1989]. The design and simulation of a multiplier block for a high speed digital filter is given here as an example of a larger circuit.

6.5.1 Digital filter

A high-speed digital equalization filter for use in the demodulation circuit of a satellite receiver compensates for imperfections in the transmission path from a sending earth station, through the satellite, to the receiving station. At present, it cannot be implemented with commercial integrated circuit technologies because data rates are too high (120 Mbit/s). The challenge is to design the filter element with the high speed potential of Gallium Arsenide digital integrated circuit technology.
The digital filter element consists of a multiplier, adder and delay block as shown in Fig 6.9 [Tewksbury et al. 1987]. Careful design of the multiplier is the most important task in the filter implementation. A serial architecture can achieve the desired data rate and the delay function is inherent in the serial multiplier. The co-efficients remain constant. A two’s complement multiplier is suitable because it is immune to overflow and automatically scales the product to the same number of bits as the input stream [Pekmestzi and Papadopoulos 1974]. The multiplier consists of identical blocks as shown in Fig 6.10 and 6.11. The control line bit is a logical one for all data bits except the most significant bit for which it is zero. The last block in the multiplier can be adapted to perform the addition function in the filter element.

![Figure 6.10. Complete serial multiplier made by repeating the one-bit block shown in Fig 6.11. The switch control inputs, \( s_i \), are set to 0, 1 or \( y_o \) as indicated. Note that the last block has an inverted \( x \) input.](image1)

![Figure 6.11. Basic block of the serial multiplier.](image2)
Figure 6.12. Standard gate implementation of serial multiplier block. The gates labelled ‘M’ are twice the size of the others. The thicker lines are the nodes shown in Figs. 6.13 and 6.14.
6.5.2 Circuit Design and Simulation

Fig. 6.12 shows a single multiplier block designed with gates from the standard gate library. Complementary logic levels are maintained throughout the design to eliminate inverter delays. Exclusive-or functions are performed with two NAND/NAND gates using and providing complementary signals. The high-power gates (labelled $M$ in the circuit) are used in large fan-out situations.

The circuit is designed for a 120 Mbit/s (125.83 MHz) data stream. A 1510 MHz data stream results when sampled at 2 samples/bit with a 6-bit analog-to-digital conversion. Simulation of this circuit at 1.6 GHz shows correct operation so the data rate can be achieved (Fig 6.13). At 2 GHz, the ‘carry out’ fails as shown in Fig 6.14.

**Simulation**

The performance of the switched network model is demonstrated by the simulation of the serial multiplier block. As shown in Figs. 6.13 and 6.14, the switched-linear network model is in excellent agreement with the device-level SPICE simulation and is able to reproduce accurately the glitches which occur before the outputs finally settle. In particular, the failure of the ‘carry out’ latch to toggle (circled region in Fig 6.14) is simulated in the same way with both models. The ‘carry’ signal at the input of the latch changes too late to set-up the latch.

This circuit consists of 51 gates and the normal SPICE simulation is performed with a 271 node circuit on a SUN 4 in 2346 seconds of CPU time. The equivalent switched-linear network scheme using SPICE switch elements consists of 2107 nodes and runs in 1056 seconds which is a 220% increase in speed.

In normal use the switched-linear network models would be used in a scheduler such as the Simulation Jig [Dunn 1989] which is a mixed-mode (analog/gate-/behavioural) simulator. The implementation in a scheduled set of computer code modules (rather than SPICE switches and linear elements) will run considerably faster because the simulator is more efficient and there will be fewer circuit nodes†.

† A typical SPICE simulation time is proportional to $n^\eta$ where $n$ is the number of nodes in the circuit and $\eta$ is a constant near 1.4. If each switched-linear network is implemented as a single element, rather than as several switches and devices, there would be only 130 nodes in the simulation. The expected simulation time would be $1056^* (130/2107)^{1.4} \approx 21$ s which is more than a 100 times increase in speed over the normal device-level simulation time of 2346 s.
### 1.6 GHz Timing Diagram

**Figure 6.13.** 1.6 GHz timing diagram of the multiplier block shown in Fig. 6.12. The dashed lines are from a reference SPICE simulation and the solid lines are from a switched-linear network simulation. Note that the X and Control signals are probed in the centre of their shift registers.

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### 2.0 GHz Timing Diagram

**Figure 6.14.** 2.0 GHz timing diagram of the multiplier block shown in Fig. 6.12. The dashed lines are from a reference SPICE simulation and the solid lines are from a switched-linear network simulation. Note that the X and Control signals are probed in the centre of their shift registers.

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6.6 Summary

This chapter has presented a new logic gate simulating technique called Switched-Linear Network Modelling and has described how to extract the models using SPICE. An example of the performance of the modelling technique has also been presented.

The switched-linear network models give an accuracy comparable with that obtained from SPICE device-level models. At the same time it requires far less computational effort in simulation, allowing the investigation of larger circuits.

Computational efficiency and accuracy are achieved simultaneously by a scheme which switches between a small but sufficient number of networks of linear grounded elements in order that all relevant regions of gate operation are modelled. A careful analysis of gate operation provides the basis for defining the relevant operating regions.

The procedure described for extracting models directly from a device-level SPICE description and simulation has been automated using SPICE3. This automation also guarantees accuracy.

The structure of the models automatically accounts for variation in fan-in and fan-out loading. This is because each element supplies the correct loading capacitance and the component values are dependent upon both the input and output nodes.

The technique has been developed and demonstrated for BFL GaAs MESFET circuits. However, it is clear that it can be applied to the modelling of high performance circuits using other logic families, technologies or devices. The merit of the technique for each case would depend on the number of networks needed for accurate simulation.

A significant benefit gained from the process of extracting the model is insight into the detailed operation of the individual gate elements. For example:

- The delayed response of the buffer stage to a falling input is caused by charging of the source follower’s gate-source junction.
- The source node of the pull-up transistor in the logic stage is sensitive to capacitance loading.
- The lower input of a dual gate switch has a slower response to a rising input because the upper gate junction must be charged. This is equivalent to a drain loading so a faster input rising edge cannot necessarily decrease the response time.
6.6.1 Chapter 6 References


7 Automatic Design from Device to Circuit Libraries

7.1 Introduction

The major part of the development of a digital circuit design capability is the creation of re-usable resources including models and libraries of devices, logic gates and common standard cells. The continuing evolution of the CSIRO fabrication process has dictated a resource development approach that readily accommodated change. This was a primary theme in the model extraction process and gate design scheme presented Chapters 4 and 5. This chapter describes the design system which brings together the processes for creating circuit design resources automatically. Automation is possible because of the development of the gate design procedure and switched-linear network schemes which can be implemented in an unsupervised computer program.

The overall design system presented in this chapter analyses fabrication process information to produce standard cells as a set of model descriptions and mask layouts suitable for assembling and simulating circuit designs. The design system is the logical end-result of the research project and has been reported at the 1989 Gallium Arsenide Symposium [Parker et al. 1989].
7.2 The Fundamental Starting Point

The design system commences with the fundamental physics of the material and properties of the fabrication process. This gives an ability to rapidly adapt to the evolving fabrication process and provides three benefits:

Firstly, because the design sequence is automated, a change in the fabrication process can be painlessly entered to update an entire circuit library.

Secondly, the design sequence starts at a level that allows it to be readily adapted to a significant change such as a change of material, from GaAs to InP for example. Also, additional model descriptions can be added to the system to accommodate a move from MESFET to HEMT technology. This means that this work can be directly applied to a new technology as the need arises.

Thirdly, the design system becomes a valuable tool for determining the effect of process variations on the final circuit elements. The existence of good models allows the designer to verify circuits. The dependence of the model parameters on material and process properties allow the investigation of the effects on the circuit of device variations and fabrication tolerances. In addition, if a fabrication process modification is planned its effect on the digital library can be quickly assessed.

7.3 Design Tools and Standard Libraries

Fundamental to the digital circuit design process is the set of CAD tools used to assemble and simulate circuits. Simulation tools in the design system use the device and circuit models described in Chapters 3 and 6, and layout tools use the fabrication design rules given in Appendix section 9.1.2.

7.3.1 Circuit Simulation Models

A single model is not adequate for every application. Determination of device characteristics from material and process properties requires a detailed model based on the device physics. Small custom cells and circuits are best designed using discrete device models with the aid of an accurate device-level circuit simulator. Larger circuits require more efficient gate-level models. Three levels of modelling are necessary.
Physical-Level Model

Accurate analytic models which consist of computationally intensive implicit equations and even two-dimensional analysis [Shur and Eastman 1978, Pucel et al. 1975] have been reviewed in Chapter 2 section 2.3.2. These models are not suitable for general circuit simulation but rather for the analysis of the single device. The results and approximations from the Pucel et al. [1975] model have been used in Chapter 4 as the basis for determining parameters for simpler models.

Device-Level Model

The SPICE [Quarles 1989] circuit simulator uses device-level models suited to the simulation of small circuits. Accurate and rapid simulation is provided by the existing device models and the new MESFET models presented in Chapter 3. Second-order effects and careful matching of the small-signal models have produced reliable models that can be used as a substitute for a fabrication test run. The device models are available for designing custom circuits and for the development of gate-level models. These models including parasitic elements are also arranged in subcircuits to form a library of standard cells.

Gate-Level Models

The Simulation Jig [Dunn 1989] is a mixed-mode (analog/gate/behavioural) simulator. It is ideally suited to the implementation of gate-level models including the switched-linear network models developed in Chapter 6. This provides a rapid simulation of large circuits.

7.3.2 Circuit Layout

The mask layout tool, Magic [Berkeley, 1986], includes design rule checking and circuit extraction functions. It can be used to lay out custom circuits (including library cells) and assemble cells from the circuit library. The design rules for the fabrication process are used by the Magic checking and extraction routines.
7.3.3 Cell Libraries

The CAD tools draw on a library containing cell models and layouts. The library includes a standard set of logic functions with a range of power and speed characteristics. Each library element is represented in three forms: a device-level model based on discrete devices, a gate-level model for rapid large-circuit simulation, and a mask layout description. Also available is a set of discrete device models for the design of custom elements and for use with the library gate-level models.

7.4 Design System Implementation

The design system is the bridge between the fabrication process and the set of device model descriptions, standard cell models and standard cell layouts. The core of the system is a PC-based front-end software package, GaAsSPICE, which maintains a database and provides an interface for designer interaction. Additional packages produce switched-linear network models and cell masks (Fig. 7.1).

7.4.1 The Design System Features

The design system follows a logical design flow from fundamental parameters through to an automatic design of logic gates. Design commences with the input of fundamental material and process parameters and design rules. Sensible default parameters are available at all stages so that the designer may take up the design sequence at any stage. This means that experimenting with and learning the design procedure can be carried out without detailed knowledge of the actual fabrication process.

At the same time, the system is structured so that it is possible to by-pass the fundamental steps and introduce parameters which more closely resemble the current fabrication performance. Moreover, derived (calculated) values may be overridden by those obtained from measurement. If the process is known, the appropriate parameters can be entered and device models will be generated. If measured device parameters are available, the process parameters can be by-passed and the design sequence started with entry of the device descriptions.
7.4.2 GaAsSPICE

The GaAsSPICE program was written to fulfill the requirement of a rapid design system for GaAs BFL Gates. It was originally intended to be an aid for determining the necessary SPICE device model parameters from the GaAs process and material properties, hence GaAsSPICE. The addition of automatic file preparation and then the design of logic gates proved to be worthwhile and expanded the concept of GaAsSPICE considerably. All this is done using a standard Spreadsheet program on a personal computer.

Operation

The operation of the GaAsSPICE program is shown in its user manual, reproduced in Appendix section 9.3. GaAsSPICE has a highly modular structure in which a main engine invokes separate script files and calculation routines as needed. This flexible arrangement isolates independent design activities and facilitates rapid change of the design steps. For example, changes in circuit topology or subcircuit requirements are made simply by updating the appropriate script file. New simulators are accommodated by changing the parsing script to produce models in an appropriate format.

GaAsSPICE performs a triple set of calculations to give models for a nominal condition and two extremes of logic levels. The calculation of these extremes has been described in Chapter 5 section 5.5.
The flow of the program is shown in Fig. 7.2. The operation can be divided into two sections: the determination of device characteristics and model parameters and the design of the basic logic gate using the available devices.

**Generation of Device Models**

The extraction procedure developed in Chapter 4 is used to create the SPICE model cards. The procedure is initiated with the basic properties of GaAs material, properties of the fabrication process and the device dimensions. These parameters are entered in three stages corresponding to the classification given in Chapter 4 section 4.5.1: the first for material properties, the second for process parameters (which are constant for a given process) and the third for design parameters. The designer can enter the system at any stage and earlier stages will use sensible default parameters.

*GaAsSPICE* then automatically generates accurate SPICE analog device model parameters suitable for use in the design of both linear and digital circuits. The user can enter the device characteristics or allow *GaAsSPICE* to calculate them from the fundamental parameters. Specifically, the diode and MESFET model parameters are listed.
with an option to override each.

All material and process parameters have associated tolerances or bands of variation. These are used to create models at the extremes of process variation and operating environment. GaAsSPICE takes these parameters and builds three models representing two extreme and the nominal devices. The designer can override the nominal result and new extreme cases are automatically calculated as a deviation from the entered nominal model as described in Chapter 4 section 4.5.1.

*Gate Design.*

An interactive gate design routine is used to produce a reference logic gate. The extreme of logic levels expected with process and environment variation are graphically given so that the user can check that the design parameters result in an effective circuit over all process and environment tolerances. The design procedure developed in Chapter 5 is used. This considers designer specified power/speed trade-offs and constraints on specification of power supplies, logic swings and nominated fan-out. The sequence produces a template for a family of logic gates.

The simple piecewise linear device models used in the gate design procedure can be calculated by the program using the model parameters it determined. Alternatively, they can be obtained by using SPICE to produce characteristic plots of the devices and then entering the parameters measured from the plots. Of course, the measured characteristics of real devices can be used.

*Library Generation*

The final step creates the SPICE ‘include’ files of gate libraries and model cards for various process settings and, additionally, produces a set of parameters which can be used by other processing routines to generate the switched-linear network models and layout cells.

A logic gate library is generated automatically by a parsing routine from the template which gives the rules for determining the relative widths of devices in the BFL gate as described in Chapter 5 section 5.6. A family of gates is created by different combinations of dual and single gate switches. Also, different power and fan-out families are generated by scaling the gates and altering the relative size of the buffer and logic stages.
7.4.3 Switched-Linear Network Models

Gate-level models are produced with a SPICE3 script program that instructs SPICE to probe each device in its actual operating environment within the basic gate template. The raw data is then ported to a formatting routine to produce the switched-linear network models as described in Chapter 6. The formatting routine can produce C-code routines for use with the Simulation Jig [Dunn 1989] or similar logic simulator. Alternatively, for the purposes of testing, the model is built up using SPICE circuit elements and switches.

7.4.4 Mask Layout

A layout package uses the basic gate template produced by GaAsSPICE to automatically create CIF cells for each circuit in the model library. The cells follow a standard layout and the relative size of each component is adjusted as required. These cells are assembled manually with Magic and a set of process design rules is used for layout checking and circuit extraction. The parasitic capacitance and resistance elements are extracted from the geometry of the final layout with the equations developed in Chapter 4 section 4.2.

7.5 Experimental Verification

The verification of the design system with experimental results proved to be quite difficult for several reasons. Firstly, the production rate of the processing facility was low and only two mask sets were fabricated during the project. Therefore, there is no valid statistical data on the variation of the process. Secondly, an etch uniformity problem with the fabrication process inhibited the investigation of small devices and circuits. Thirdly, the task of measurement is difficult at the gigahertz frequencies involved principally because, even though a sophisticated probe station and test equipment were available, the 50 Ω loading imposed by the instruments is considerable.

Despite these problems operation of an inverter to 5 GHz was confirmed and simulated predictions matched with Voltage Contrast Microscopy measurement. The following paragraphs give a concise summary of the experimental results and compares them with predicted performance. A more detailed description of the testing procedure and results is given in Appendix section 9.1.
7.5.1 High Speed Measurement

High frequency performance of the inverter circuits on the second mask was tested with a Hewlett Packard HP 8510 network analyser, a signal generator, a sampling oscilloscope and a Cascade Microtech microwave probe station. Significant losses in the cables and probe heads were difficult to quantify so the amplitudes of the signals involved have large error estimates (±15%). The measurements made on the medium size (36 μm) inverter in chip M-2(3)J are shown in Appendix section 9.1 Photos 9.8, 9.9 and 9.10 for 2.5 GHz, 4.5 GHz and 5.5 GHz. Operation of the inverter deteriorated rapidly beyond 5.5 GHz and the output amplitude dropped to a residual non-inverted signal. Reasonable agreement with the measurement was achieved within the measurement error estimates. More detail is included in Appendix section 9.1.7 and an example simulation is presented in the GaAs IC symposium paper [Parker et al. 1989].

The circuit was designed using the procedure reported in Chapter 5 with the assumption that each device is identical except for width. However, the fabrication process reduced the pinch-off potential of the narrow devices as shown in Appendix Fig 9.4. Also, the circuit was fabricated before the completion of the full design system and was laid out by hand with an ohmic contact geometry which varies between devices. Accounting for the variations in pinch-off potential and geometry was necessary in order to match prediction with theory. An adjustment to the models of each device in the inverter circuit was made on the basis of the relation of pinch-off potential to device width determined by measurement of individual devices on the chip and an adjustment to the parasitic element values was made on the basis of the actual layout. It should be noted that with an improved etching technique and uniform layout this adjustment would not be necessary. The device model parameters used are given in the SPICE listing on the following page.

7.5.2 Voltage Contrast Microscopy

Because of the uncertainty of the probe measurements and fabrication procedure, an alternative method of verifying the circuit operation and the design procedure was sought. This was provided by Telecom Australia at their Research Laboratory (TRL). The author designed and constructed a suitable test jig and travelled to TRL to make the measurements with the assistance of the Device Technology Section’s Principal Physicist, Dr. Tim Rogers.
This SPICE deck is given for the model cards and circuit description for 36 um inverter circuit tested with voltage contrast microscopy.

---

**MODEL Cards**

These are MESFET, Diode, and capacitance models for 1 micron wide devices. The pinch-off potential and resistances vary between devices.

- **.MODEL Mpd NJF**
  - VTO= -2.75
  - Beta= 154u
  - Eta= 49m
  - XI= 0.12
  - pb= 0.7
  - RS= 500
  - RD= 1400
  - Lambda= 76m
  - CGD= 0.08f
  - CGS= 2.13f
  - Kappa= 0.36
  - Theta= 8
  - cmod= 2

- **.MODEL Mpf NJF**
  - VTO= -2.25
  - Beta= 166u
  - Eta= 49m
  - XI= 0.14
  - pb= 0.7
  - RS= 970
  - RD= 1400
  - Lambda= 76m
  - CGD= 0.08f
  - CGS= 2.13f
  - Kappa= 0.36
  - Theta= 8
  - cmod= 2

- **.MODEL Schottky D**
  - IS= 7599f
  - Rs= 1600
  - N= 1.19
  - CJO= 4f
  - VJ= 0.7
  - BV= 9.4

- **.MODEL Cds C**
  - CJ= 0.067ff
  - CJSW= 0
  - DEFW= 1

- **.MODEL Cgs C**
  - CJ= 0.087ff
  - CJSW= 0
  - DEFW= 1

- **.MODEL Cgd C**
  - CJ= 0.087ff
  - CJSW= 0
  - DEFW= 1

---

**Power Supplies**

- **Vvdd vdd 0 4V**
- **Vvss vss 0 -3V**

---

**The inverter and parasitics**

- **jswitch sfgate input 0**
- **Cdsaw sfgate 0**
- **Cgsaw input 0**
- **Cgdaw sfgate input**
- **jpullup vdd sfgate sfgate**
- **Cdspu vdd sfgate**
- **Cgpdu vdd sfgate**
- **jsf vdd sfgate sfsource**
- **Cdsff vdd sfsource**
- **Cgsff sfsource sfsource**
- **Cgdaf sfsource sfsource**
- **dtop sfsource anmid Schottky 127**
- **Ctop sfsource anmid**
- **dmid anmid anbot Schottky 127**
- **Cmid anmid anbot**
- **dbot anbot output Schottky 127**
- **Cbot anbot output**
- **jpull vdd sfsource output vss vss**
- **Cdspd output vss**
- **Cgdpd output vss**

---

**Smoothed pulse input**

- **vinput xin 0**
- **pwl 0 -1.3 0.7n -1.3 1.4n 0 4n 0 4.7n -1.3**
- **rin xin ein 2k**
- **cin ein 0 50f**
- **ein input 0 ein 0 1**

---

Chapter 7: Automatic Design from Device to Circuit Libraries

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The high-speed and dc measurements were carried out with a non-invasive Voltage Contrast Microscope as described in the appendix. A 730±10 ps sampling gate is used and a computer analyses the image to build up an oscilloscope-style display of the potential at the image point. The measurements are shown in Figs. 7.3 and 7.4 together with a SPICE simulation. The effect of the sampling gate width was included by convolution of the signal data produced by the SPICE simulation with a 730 ps window. The agreement with timing and dc levels is very good.

Figure 7.3. Measured falling transition of an inverter. The SPICE simulation convolved with a 730 ps gate window is shown by diamonds and the voltage contrast measurements are shown by the lines.

Figure 7.4. Measured rising transition of an inverter. The SPICE simulation convolved with a 730 ps gate window is shown by diamonds and the voltage contrast measurements are shown by the lines.
7.6 Summary

The design system ties together all the major results of this thesis into a single CAD package. It commences with input of the fundamental process parameters and design rules. From these, SPICE models suitable for use in the design of both linear and digital circuits are automatically generated. These, in turn, are used to automatically design and lay out basic logic gates. Simplified models of the gates are extracted for use with a mixed-mode simulator. The design sequence is automated and can be easily repeated under the control of the PC-based front-end software package, GaAsSPICE. The modular structure of this package facilitates rapid change of the design steps. Thus, it will be a useful aid in the rapid application of new technologies.

An important feature of the program is an ability to override its internally calculated quantities with measured results and to provide default parameters. This ability allows the designer to take up the technology at different levels. Starting without a fabrication process in mind the designer can explore the devices and perform feasibility studies. As the process materialises, the parameters calculated in the program can be substituted with more precise detail. It can be adapted quickly to a fundamental change in technology and therefore is a valuable tool for determining the merits of a process modification.

The facilities developed for the design system have been used to fabricate a working inverter which has demonstrated operation above 5 GHz. Also, the operation of the inverter has been accurately simulated with the design system generated models (after accounting for processing problems and noting that an early lay-out procedure was used).
7.6.1 Chapter 7 References


8 Conclusion

The project reported in this thesis has achieved its goal of establishing a base for a GaAs logic circuit design facility tailored to the anticipated Australian capability. Although special consideration has been given to the use of the low noise fabrication process being developed at the CSIRO Division of Radiophysics, a significant achievement is that the process of establishing the resources for the design facility has been assembled into a design system which can be used to perform the same task with new technologies. The impact of this project is therefore a long term one which will allow the design facility to keep pace with technological development.

Moreover, developments ancillary to the main aim of the project form a solid base for new areas of research and development. Notable achievements are an improvement to the SPICE JFET model, an extension of this JFET model to accommodate MESFET's accurately, the development of an automatic system for designing basic logic gates and the development of a switched-linear modelling technique which features the ability for automatic extraction of the models.

8.1 Developed Resources

The tools and resources for the GaAs digital design facility have been established in four categories; firstly, device models for accurate simulation of both analog and digital circuits; secondly, a technique for the simulation of a large digital system; thirdly, a design procedure for generating a library of basic logic circuits; and fourthly, a procedure for extracting model parameters from fundamental material and fabrication process parameters.
8.1.1 Device Modelling

The SPICE circuit simulator was chosen for device level modelling because it is suitable for mixed microwave analog and digital circuits. Shortcomings of the existing MESFET models have been addressed with the development of a new unified JFET/MESFET model. This gives the designer an accurate MESFET and JFET model which can match small-signal behaviour over an extended range. Unlike other models, the unified model can accommodate FET’s of any gate length which is a significant advantage for mixed analog and digital applications. It provides a ‘doping profile parameter’ to adapt correctly to various doping profiles and provides the second-order and capacitance effects observed in real devices. Parameters are provided to fit the observed second-order effects of pinch-off potential modulation and its ac dependency, channel-length modulation and the reduction in drain-source current (due to temperature or electron velocity effects).

8.1.2 Switched-Linear Network Modelling

For the purpose of simulating large circuits a new switched-linear network modelling technique has been developed. The technique is a significant improvement over existing timing models especially for time critical applications. Switched-linear network models are computationally efficient yet give an accuracy comparable to that obtained with device-level SPICE models. They predict the finer details of signal transition important in high performance Gallium Arsenide circuits which are pushed to their limit. Accuracy is achieved by switching between a number of linear networks which model all regions of gate operation. The structural basis of the models inherently accounts for gate loading. This permits accurate and, most importantly, automatic extraction from a device-level SPICE simulation.

8.1.3 Circuit Design

An automatic design procedure which generates a family of logic functions with various power and speed capabilities has been developed. Useful results are obtained from a simple piecewise-linear transistor model. The simplicity of the procedure allows it to be used for checking gate design at the extremes of process variations. The resulting gate design is structured as a template for the automatic generation of a standard logic cell library.
8.1.4 Device Model Parameter Extraction

The main path between the fundamental material and process parameters and detailed models is the procedure developed for the extraction of the SPICE model parameters. Where possible, each parameter has been derived through basic theory in terms of fundamental properties or to fit a reference model. This allows determination of the variation of each parameter with each property and extraction of circuit characteristics from layout geometry. Some new approaches and improvements are the following:

**Capacitance.** Improved expressions for coplanar and ground capacitance have been developed which consider a wider range of geometries.

**Diodes.** The SPICE diode model is used by selecting suitable model parameters to adapt the silicon based model to GaAs. A new interpretation of the diode description predicts an emission co-efficient (ideality factor) greater than unity as in real devices. The reverse leakage current is calculated from the population of electrons in the metal using their mass in the metal rather than the semiconductor. Also, a suitable model of diode planar effects which uses two ideal diodes in series has been explored.

**MESFETs.** A system for determining MESFET model parameters based on the Pucel et al. model is used for determining the parameters for the existing SPICE models as well as the new unified model. The second-order effect parameters are also determined with an analysis applicable to short channel devices.

**Automatic Design from Device to Circuit Libraries.** The procedures developed for the project have been brought together into a computer based design system which is the bridge between the fabrication process and the set of model descriptions, standard circuit elements and layout cells. The core of the system is a PC-based front-end software package, *GaAsSPICE*, which maintains a database and provides an interface for designer interaction. The design system follows a logical design flow from fundamental parameters through to an automatic design of logic gates. Flexibility is achieved by providing sensible default parameters at all stages and allowing all derived parameters to be overridden.

*GaAsSPICE* has a highly modular structure which allows independent design activities and facilitates rapid change of the design steps. It performs a triple set of calculations to give models for a nominal condition and for two extremes cases of logic levels, it creates gate libraries and model cards for various process settings and it produces a set of parameters which can be used by other processing routines to generate the switched-linear network models and layout cells.
The automation of the design system provides three main advantages. Firstly, a change in the fabrication process can be re-applied easily to update the developed resources. Secondly, it can be adapted quickly to a fundamental change such as a change of material. Thirdly, it can serve as a tool for the appraisal of fabrication changes.

*Design Rules.* A conservative set of circuit layout design rules which consider limitation of lithography, alignment, processing and electrical design has been developed in consultation with the CSIRO. The rules were subjected corrections and enhancements based on experience with fabricated chips. In addition, the following physical properties of circuit devices are used to derive layout rules.

– The salient property of an ohmic contact is the contact’s transfer length which quantifies the practical design limit on its length.

– The capacitance between parallel conductors is used to determine their minimum spacing.

– The maximum length of the diode is set to avoid planar effects which cause increased resistance. This limit is chosen so that a twin diode model is not necessary.
8.2 Ancillary Developments

8.2.1 Logic Family Design

*Circuit Analysis and Modelling*

The switched-linear network modelling technique has the additional benefit of being a valuable method for studying the exact operation of a circuit. The exact structure of a switching model is found by considering each element in the logic gate and its influence on the external nodes of the gate. It is this method that isolates and highlights the critical components and their effects on the circuit giving clear insight into its operation.

While the technique has been developed and demonstrated for BFL GaAs MESFET circuits it is clear that it can be applied to the modelling of high performance circuits using other logic families, technologies or devices. The merit of the technique for each case would depend on the number of the networks needed for accurate simulation.

*A New Logic Family*

The buffered logic topology is improved with the use of a *Swing Limiter* diode. A new logic topology called Saturated Buffered FET Logic is proposed which uses a Swing Limiter diode to limit the logic transition at the input of the buffer stage. It is worth noting that this improvement was discovered through the study of the gate circuit during the preparation of the switched-linear network models.

The use of the Swing Limiter diode can be extended to any application where a source follower buffer is used. The speed of a SBFL ring oscillator can be up to twenty percent faster and has lower power consumption. There is no reduction in the noise margin and the additional wafer area required to accommodate the *Swing Limiter* diode is less than three percent of the total area of the gate.

8.2.2 Design Environment

The *GaAsSPICE* program is implemented on a PC based system. This provides an inexpensive front-end which is very easy to modify as the technology changes. The sys-
tem is also a valuable training tool which allows designers to experiment with gate
design and circuit properties. This approach should be of benefit to other areas of circuit
design.

8.3 Further Research Opportunities.

The design system and modelling techniques form a solid basis for further work beyond the scope of this thesis.

8.3.1 Further Fabricated Circuits

The programme of research for this thesis has been dictated by the limitations imposed by the availability of resources and experimental data. A limited amount of experimental verification has proved useful and the basic predictions of the simulation system have been confirmed with measurement. However, there are aspects of the design such as the minimum width limit of narrow devices which require experimental investigation. At present a fabrication process etching problem appears to limit the performance of narrow devices. The elimination of this problem is being investigated so that a reasonable test of device scaling can be performed.

8.3.2 Analog design

Several types of custom circuits are required for specific applications. Many require analog capability or front-ends before digital processing can be performed. Operational amplifiers, line drivers, pad drivers, optical interfaces and logic level shifting applications are areas which will require analog design techniques. The unified MESFET model is an excellent tool for this sort of analog design and has been used in the development of a high performance operational amplifier [Barnes et al. 1989].

Microwave Amplifiers

The ability of the improved JFET model and hence the unified model to give a better match to small-signal behaviour is significant for the simulation of microwave analog and power amplifiers. A landmark ability will be the correct prediction of third-order intermodulation products which the traditional square-law models cannot produce.
**Further Investigation of Second-order Effects**

Second-order effects required for adequate MESFET simulation of depletion mode logic have been included in the unified model. However, there are other effects such as breakdown, drain-source punch-through and sub-threshold leakage current which are significant in power amplifiers and enhancement mode devices. Preliminary work on adding these effects to the unified model is giving promising results.

**8.3.3 Adaptation to Emerging Technologies**

The emerging High Electron Mobility Transistor (HEMT) which offers higher speed and better noise performance than the conventional GaAs transistor can be accommodated in the design system. The provision of a suitable SPICE model is already under investigation as part of another project [Mahon and Skellern 1989]. In the longer term, the inclusion of Heterojunction Bipolar transistors and other devices can also be considered.

**8.4 Applications for the Design Facility**

The applications identified as most suitable for the Australian fabrication capability are those which require the integration of both analog and digital functions on the one chip. There are relatively small circuits such as analog-to-digital converters, frequency dividers and synthesizers which can be easily accommodated with an analog circuit. An example of a digital filter element has been given in Chapter 6. Other areas include high-rate switched capacitor systems using operational amplifiers similar to the one developed by Barnes et al. [1989].

The development of the design system and the resources in this project have brought the Australian capability to a position where the development of signal processing circuits is feasible. Most importantly, the ground work for further development is set and the ability to keep pace with technological advance has been included.
8.5 Chapter 8 Reference


9 Appendix
9.1 Fabricated Test Circuits

Experimental results presented in this thesis were obtained from chips manufactured by the CSIRO Division of Radiophysics. Relevant results and demonstrations have already been given in appropriate sections in the previous chapters. This appendix section gives more detail on the chips fabricated and how the measurements were made. Results not given in the previous chapter are also presented.

9.1.1 Introduction

During the project two mask sets were fabricated. These have been designated M-1, M-2(1), M-2(2), and M-2(3) where the parenthesized numbers refer to three productions of the second mask. Each mask included several identical chips designated A, B, C,... and the number of chips varied in each production depending on the size of the wafer.

9.1.2 Mask Preparation

The design rules used in the preparation of the optically generated masks are defined in terms of design rule parameters listed in Table 9.1. These were devised in consultation with the CSIRO Division of Radiophysics. The minimum feature size was normally limited by the mask making process at AWA Ltd in 1987 to 2.5 μm but thinner lines, down to 1.25 μm, have been produced at extra cost by adjusting exposures.

Test structures for determining ohmic contact performance, checking other process dependent parameters and testing discrete devices have been included in each mask. These are based on the diagnostic pattern proposed by Immorlica et al. [1980]. Material evaluations were carried out by the CSIRO, so Hall-effect tests and profile checks were not included in these masks.
Table 9.1. Design Rules for Mask Preparation.

- δ = 0.5 μm alignment registration limited by ability to align mask layers,
- φ = 0.25 μm enlargement of metal layers which occurs during their deposition,
- λ = 2.5 μm minimum line width limited by mask making process,
- s = 0.5 μm width of mesa side wall caused by undercut during etch process,
- D = 4.0 μm minimum feature spacing limited by surface leakage,

<table>
<thead>
<tr>
<th>Mask Type</th>
<th>Rule Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mesa Mask</td>
<td>Minimum mesa to mesa isolation D+2s = 5 μm</td>
</tr>
<tr>
<td>Ohmic Mask</td>
<td>Ohmic metal contacts should be inside mesa outline by δ+s+φ = 1.25 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum ohmic line width 2δ+λ+2φ = 4 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum spacing metal to metal D = 4 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum spacing metal to mesa D = 4 μm</td>
</tr>
<tr>
<td></td>
<td>A connection to Schottky metal can to come within 4s = 2 μm</td>
</tr>
<tr>
<td>Schottky Metal Mask</td>
<td>Minimum gate to ohmic spacing 2δ+2φ = 1.5 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum extension of gate over mesa 4s = 2 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum Schottky to ohmic contact area 8 μm²</td>
</tr>
<tr>
<td>Gold Overlay Mask</td>
<td>Minimum gold line width λ = 2.5 μm</td>
</tr>
<tr>
<td></td>
<td>Gold overlay should be inside ohmic metal outline by δ+φ = 0.75 μm</td>
</tr>
<tr>
<td>Air-bridge Base Mask</td>
<td>Minimum gold bridge base width should be λ+2φ = 3 μm</td>
</tr>
<tr>
<td></td>
<td>Gold bridge-base should be inside gold overlay outline δ-φ = 0.25 μm</td>
</tr>
<tr>
<td></td>
<td>Minimum Bridge-base to first level wiring spacing 3+δ = 3.5 μm</td>
</tr>
<tr>
<td>Air-bridge Mask</td>
<td>Minimum bridge width λ+2δ = 4 μm</td>
</tr>
<tr>
<td></td>
<td>Bridge should be outside gold bridge-base outline d = 0.5 μm</td>
</tr>
<tr>
<td></td>
<td>Maximum air-bridge span 50 μm</td>
</tr>
</tbody>
</table>

Photo 9.1 An example of destructive testing of a dual gate MESFET.
9.1.3 Fabrication Data

Mask-1

Fabrication Date: June 1987

Chip Count: Four chips (M-1A, M-1B, M-1C, & M-1D)

Structures: Material and design diagnostic pattern, lithography tests, a basic BFL gate, CCFL test structure, air-bridge structure and a full adder.

Process Notes: Gate line width was 2 \( \mu \)m.
An MBE grown epi-layer with \( 2 \times 10^{17} \text{ cm}^{-3} \) doping was used.

Outcome: The aspect ratio of the diodes in the BFL circuits was near square so the diodes exhibited significant planar effects. Therefore the circuits did not function correctly because of excessive potential across the diodes.

The Mask set was useful for refining the design rules for metal run-out and mesa undercut and for adjusting the alignment marks and air-bridge formation.

Recommendations: The geometry of diodes should be changed in the next mask so that the increased potential drop due to planar effects is reduced.

Photo 9.2 shows the overall pattern of chip M-1D. Features can be identified with the aid of the schematic in Fig. 9.1.
Appendix: Fabricated Test Circuits

Mask-2 run 1

Fabrication Date: July 1988
Chip Count: Nine chips [M-2(1)A, M-2(1)B, ..., M-2(1)I]
Structures: Material and design diagnostic pattern, lithography tests, a basic BFL gate, capacitor coupled FET logic (CCFL) test structure, air-bridge structure, a full adder and a sample-and-hold circuit.

Photo 9.2. Optical Microscope detail of chip M-1D. Each bond pad is 100 μm square.
Process Notes: Gate line width was 1.5 \( \mu m \).
A vapour grown epi-layer with \( 2 \times 10^{17} \) cm\(^{-3} \) doping was used. A new three step (1500 Å, 1500 Å, 2000 Å) mesa etching process was used to reduce undercut and give gentle slopes in all four directions.

A longer exposure was used with the ohmic metal wiring mask as an attempt to join an erroneous 0.5 \( \mu m \) gap where some of the mask lines should have met.

Outcome: Unfortunately the devices were pinched off so it will be necessary to reduce the recess etch in the next wafer. Those devices which did operate exhibited a high drain-source resistance and non-uniform transconductance characteristic due to the tail in the doping of the material used. Dual gate lines were separated by a 1.5\( \mu m \) line of resist during the process. This proved to be too thin for the wider devices and resulted in a bulging of the gates consistent with flexing of the resist between them.

Recommendations: An MBE material with a thinner active layer would be desirable. This would reduce the mesa undercut and give an improved operating characteristic.
Mask-2 run 2

Fabrication Date: August 1988


Structures: Material and design diagnostic pattern, lithography tests, a basic BFL gate, capacitor coupled FET logic (CCFL) test structure, air-bridge structure, a full adder and a sample-and-hold circuit.

*Photo 9.3.* Optical Microscope detail of chip M-2(2)D. Each bond pad is 100 μm square.
Process Notes: Gate line width was 1.5 μm. An MBE grown epi-layer with $2 \times 10^{17}$ cm$^{-3}$ doping concentration was used. A three step (400 Å, 1800 Å, 1000 Å) mesa etch process was used to reduce undercut.

Outcome: All Schottky junctions were bad (ideality factor between 1.8 and 3) probably due to contamination during the processing.

Recommendations: The wafer should be fabricated again.

**Mask-2 run 3**

Fabrication Date: September 1988

Chip Count: Twelve chips [M-2(1)A, M-2(1)B, ..., M-2(1)L]

Structures: Material and design diagnostic pattern, lithography tests, a basic BFL gate, capacitor coupled FET logic (CCFL) test structure, air-bridge structure, a full adder and a sample-and-hold circuit.

Process notes: Gate line width was 1.5 μm. An MBE grown epi-layer with $2 \times 10^{17}$ cm$^{-3}$ doping concentration was used. A three step (400 Å, 1800 Å, 1000 Å) mesa etch process was used to reduce undercut (same as the second run).

Outcome: Inverter operation to 5 GHz was successfully demonstrated. However, the narrow devices have an extraordinarily low pinch-off potential. The problem seems to be an end-effect in the gate recess etching step. As a consequence, the small (10 to 20 μm wide) devices in the gates of the adder and shift register circuits did not function correctly.

Recommendations: The use of wider devices in circuit designs will allow the fabrication of working circuits in the short term. In the long term the use of another etching process such as Reactive Ion Etching would be desirable. A self limiting etching process is also a possibility [Chang et al. 1988].

The optical microscope picture (Photo 9.3) shows the overall pattern in M-2(2)D on the wafer. The schematic of the second mask’s layout is shown in Fig. 9.2.
9.1.4 Common Test Structures

Basic test structures including design rule checks, contact resistance checks and large MESFETs are common to both masks. The test patterns also include design rule checks, gate contacts and air-bridge formations. Photo 9.4 shows a close up of an air-bridge test structure.

Ohmic Contact Resistance

Both mask sets include a linear array of 100 μm × 100 μm probe contacts arranged with decreasing spacings of 20, 16, 12, 8 & 4 μm. These were used to determine the ohmic contact resistance. The resistance between adjacent pads was measured with a four probe technique (two probes supply current, the other two measure the potential). The measurements were made with a 1.0 mA current source which is much less than the 100 ~ 500 mA saturated current through the epi-layer.

The change in resistance with increasing spacing is due to the sheet resistance of the epi-layer, $R_s$. The extrapolated zero spacing resistance is the contact resistance of two contacts, $2R$. A typical measurement result from M-2(2)A is shown in Chapter 4 Fig 4.2. The metal-alloy contact resistance, $R_c$, alloy sheet resistance, $R_m$ and transfer
length, $L_t$, were evaluated using an end-resistance measurement as described in Chapter 4 section 4.2.1. The end-resistance of three adjacent contacts is the ratio of the voltage measured between the centre contact and one end-contact and the current driven from the centre contact to the other end-contact [Shur 1987]. The average of the ten possible end-resistance measurements of the six adjacent contacts is used. The equations used are derived from (4-1) and (4-3):

$$R_{\text{end}} = \frac{R_a(L_t/L)}{\sinh(d_o/L_t)}$$  \hspace{1cm} (4-3)

$$R_a = \frac{R_z L_t}{\tanh\left(\frac{d_o}{L_t}\right)}$$  \hspace{1cm} (4-1)

By definition of $L_t$

$$R_c = R_a L_t^2$$

(4-1) in (4-3) gives

$$L_t = \frac{d_o}{\cosh^{-1}(R/R_{\text{end}})}$$

The average values are tabulated below. The end-resistance measurement was not made with M-1. The lower epi-layer sheet resistance in M-2(1) is due to the thicker epi-layer thickness.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Epi-layer Sheet Resistance $\Omega$</th>
<th>Transfer Length $\mu$m</th>
<th>Contact Resistance $\Omega \mu$m$^2$</th>
<th>Alloy Sheet Resistance $\Omega$ sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-1</td>
<td>144 ± 1</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>M-2(1)</td>
<td>128 ± 6</td>
<td>22 ± 3</td>
<td>1880 ± 400</td>
<td>4 ± 1.5</td>
</tr>
<tr>
<td>M-2(2)</td>
<td>159 ± 4</td>
<td>14.0 ± 0.3</td>
<td>2800 ± 200</td>
<td>14.5 ± 1.5</td>
</tr>
<tr>
<td>M-2(3)</td>
<td>158 ± 5</td>
<td>13.9 ± 0.4</td>
<td>2700 ± 200</td>
<td>14.3 ± 2.0</td>
</tr>
</tbody>
</table>

**Fat Diodes**

Fat 100 $\mu$m × 200 $\mu$m diodes were included in the diagnostic patterns in case C-V profiling was required. The material had been well characterised by the CSIRO so only their electrical characteristics were checked.

Fig. 9.3 shows the electrical characteristic and theoretical fit of the 200 $\mu$m × 100 $\mu$m diode in the diagnostic pattern of M-1A. The measurement was made with a two wire technique and a curve tracer so the resistance of the probe needles and wiring is included. As expected planar effects are significant so the twin diode model described in Chapter 4 section 4.3.3 is needed to match the device. The reverse saturation current for the primary diode, $I_s = 3.85$ nA was calculated for a 100 $\mu$m × 200 $\mu$m area with
Reverse saturation current of the secondary diode, \( I_s = 1.83 \text{ mA} \), was calculated for a 50 \( \mu \text{m} \times 400 \mu \text{m} \) strip around the perimeter of the diode. The thickness and sheet resistance of the epi-layer were calculated assuming that the depletion potential was the same as the pinch-off potential, \(-2 \text{ V}\), of the MESFET with the same size gate area. The ideality factor, \( N = 1.15 \) was calculated with (4-19). A series resistance \( R_s = 8 \Omega \) to include the measuring probes gives an excellent fit to measurement typical of all the FAT diode measurements.

**Long Wide MESFET**

The diagnostic test pattern also includes a 100 \( \mu \text{m} \times 200 \mu \text{m} \) MESFET. These devices exhibit no short channel effects. The measurements conform well to theory as shown in Chapter 3 Fig 3.2 for the device from chip M-1A.

---

\[ I_s = 3.8 \text{ nA} \quad N = 1.15 \]
\[ I_s = 1.38 \text{ mA} \quad N = 1.15 \]
\[ R_s = 8 \Omega \]

---

\[ IS = A^*T^2\exp\left(-\frac{q\phi_b - \sqrt{nkT}}{kT}\right) \quad (4-18) \]

\[ N = \frac{q\phi_b}{kT} \left\{ \ln \left[ \frac{m^*mN_d}{m_em_N} \exp\left(-\frac{q\phi_b - \sqrt{nkT}}{kT}\right) + 1 \right] \right\}^{-1} \quad (4-19) \]
Short Wide MESFET

The diagnostic test structure includes a 200 μm wide MESFET with length 2 μm in the first mask and 1.5 μm in the second mask. Measurement from the 200 μm × 1.5 μm device on chip M-1A is shown in Chapter 3 Fig. 3.6. The measured characteristics of the 200 μm × 1.5 μm device on chip M-2(3)H are shown in Chapter 4 Figs. 4.10 and 4.11. The device nominal parameters listed in Table 4.1 were used to evaluate model parameters which are listed in Table 4.2. The agreement of the extracted model from nominal parameters with the actual device is very good.

Varying Gate Length FET's

A set of FET's with 1, 1.5 and 2 μm gate lengths are included to check the lower limit of the gate mask-making process (i.e. can a thin line be achieved with the optical mask system). All of these devices worked well, so it should be possible to use 1 micron gate lengths in future work. An electron beam lithography system will ultimately be used to give even shorter gate lengths.

9.1.5 Problems with Measuring MESFET's

The measurement of MESFET characteristics was not an easy task. There are side-effects such as light sensitivity, oscillations due to instabilities and temperature effects which hinder the measurement. The curve tracer characteristics of the 200 × 2 μm FET on chip M-1D with and without illumination are shown in Photos 9.5 and 9.6. When illuminated, the traps at the surface of the epi-layer between the drain and gate are activated and drain feedback effects are suppressed. In darkness the traps are able to respond to the drain potential and an hysteresis effect is present. The rate of the curve tracer sweeps also affects the characteristic.

Better measurements can be made with two power supplies and meters. One supply generates the drain source potential and two meters give the drain current and potential. The other power supply generates the gate source potential which is monitored by a third meter. The characteristics are measured by stepping one supply and sweeping the other at each step. Often the measurements are not stable which may indicate that there is an unstable oscillation present. Careful shielding and probing was necessary to reduce this problem.
A significant difference between the characteristics is observed depending on how they are recorded. When the gate source potential is stepped and then held constant while the drain source potential is swept the characteristics tend to be unstable and unrepeatable. A typical observation just beyond the saturation knee is an erratic drain current reading. At higher drain-source potentials the current reading drifts over a period of seconds toward a lower value. This is consistent with junction heating. As a result of these two effects the measurements were not reproducible.

*Photo 9.5. Characteristics of illuminated MESFET.*

*Photo 9.6. Characteristics of MESFET in darkness.*
The alternative approach of stepping the drain source potential and then sweeping the gate source potential gave reproducible results. The FET is actually pinched off while the drain source potential is stepped so any instability caused by drain characteristics is not excited by a potential change. The device is brought into operation with a constant drain source potential by sweeping the gate potential. Long term heating is reduced because the device is turned off between gate potential sweeps.

The scope of this thesis includes producing a model which can fit these observed characteristics and this has been achieved with the unified JFET/MESFET model described in Chapter 3. More work can be performed to improve the characterisation process especially for microwave power amplifier applications. The use of a pulsed measurement system may determine the ac behaviour of the current characteristics as suggested by Paggi et al. [1988].

9.1.6 A Fabrication Problem

The narrow devices in the third run of the second mask have an extraordinarily low pinch-off potential. The problem appears to be an end effect in the gate recess etching procedure. Increased etching at the edge of wide devices is not significant. However, it resulted in an increased overall etching in narrow transistors and reduced their pinch-off potential. The chart in Fig 9.4 shows that the pinch-off potential is dramatically reduced for gate widths less than 20 μm. These measurements were taken from several devices in the various test structures on the mask.

![Figure 9.4. Measured depletion potential of several FET's of various widths.](image-url)
Photo 9.7. SEM picture of a MESFET channel with the gate metal removed. The black scale at the bottom of the recess is aluminium oxide residue.

Figure 9.5. Schematic of MESFET channel shown in Photo 9.7. This structure is part of an array of MESFET’s designed to test the necessary gate metal overlap over the mesa sidewall. The device shown has a negative overlap.
The M-2(3) wafer was divided into two halves and the aluminium gates stripped from chips A-F. The SEM picture (Photo 9.7) of the recess of one stripped gate shows that the etch is not uniform. A schematic of this photo is shown in Fig. 9.5. The edge of the device has a deeper etch and therefore narrow devices are deeply etched across their entire width.

This fabrication problem has eliminated the possibility of acquiring useful information from many of the design rule checks and circuits on the second mask. When an improved etch is established, the mask can be fabricated again. The use of another etching process such as Reactive Ion Etching or a self-limiting etching process [Chang et al. 1988] would improve the uniformity of the channel.

### Table 9.2. Model Parameters for devices on Mask M-1.

<table>
<thead>
<tr>
<th>Device Properties</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>$L = 2.0 \mu m$</td>
</tr>
<tr>
<td>Doping</td>
<td>$N_d = 2 \times 10^{17} \text{ cm}^{-3}$</td>
</tr>
<tr>
<td>Barrier Potential</td>
<td>$\phi_b = 0.70 \text{ V}$</td>
</tr>
<tr>
<td>Mobility</td>
<td>$\mu = 4727 \text{ cm}^2/\text{Vs}$ (2-8)</td>
</tr>
<tr>
<td>Saturated velocity</td>
<td>$v_s = 8.389 \times 10^6 \text{ cm/s}$ (2-7)</td>
</tr>
<tr>
<td>Maximum velocity field</td>
<td>$E_m = 3690 \text{ V/cm}$ (4-28)</td>
</tr>
<tr>
<td>Maximum velocity</td>
<td>$v_m = 1.310 \times 10^7 \text{ cm/s}$ (4-27)</td>
</tr>
</tbody>
</table>

### MESFET Model Parameters

<table>
<thead>
<tr>
<th>Pinch-off potential</th>
<th>$V_{po} = -2.1 \text{ V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance Parameter</td>
<td>$\beta = 128 \mu A/\text{V}^2/\mu m$ (4-39)</td>
</tr>
<tr>
<td>Doping Profile Parameter</td>
<td>$B = 0.6$</td>
</tr>
<tr>
<td>Saturation Parameter</td>
<td>$\xi = 0.198$ (2-31)</td>
</tr>
<tr>
<td>Drain Feedback Parameter</td>
<td>$\eta = 42 \text{ mV}^{-1}$ (4-45)</td>
</tr>
<tr>
<td>Channel-Length mod. Parm.</td>
<td>$\lambda = 49 \text{ mV}^{-1}$ (4-40) and (4-41)</td>
</tr>
<tr>
<td>Velocity Reduction Parameter</td>
<td>$\kappa = 0.36$ (4-46)</td>
</tr>
<tr>
<td>Velocity Reduction Parameter</td>
<td>$\theta = 8$</td>
</tr>
<tr>
<td>Source resistance 2\mu m s-g spacing</td>
<td>$R_{ss} = 700 \Omega \mu m$</td>
</tr>
<tr>
<td>Drain resistance 2\mu m d-g spacing</td>
<td>$R_{dd} = 700 \Omega \mu m$</td>
</tr>
</tbody>
</table>

### Diode Model Parameters (17 \mu m \times 30 \mu m Schottky metal)

| Reverse saturation current D1 | $I_s = 9.8 \text{ pA}$ |
| Reverse saturation current D2 | $I_s = 2.0 \mu A$ |
| Ideality factor | $N = 1.25$ |
| Series Resistance | $R_s = 60 \Omega$ |
9.1.7 Circuit Tests and Simulations

First Mask

The capacitor coupled FET logic (CCFL) circuits were part of another project and were not tested.

A 40 µm BFL gate with a breakout between the inverter and the buffer stages was included in the first mask to check the behaviour of the gate. The transfer characteristics of the gate in chip M-1C is shown in Fig. 9.6 for various power supply potentials.

The diodes used in this gate are 17 µm wide by 30 µm long, so the planar effects described in Chapter 4 section 4.3.3 are quite severe. A two-diode model for each is required (refer Chapter 4 section 4.3.3) to match SPICE predictions with the measured

Figure 9.6. Transfer characteristics of the BFL test gate on Mask 1. A SPICE simulation using the parameters listed in Table 9.2 for \( V_{ee} = -3 \) V and \( V_{dd} = 5 \) V is shown with crosses.
The parameters used are listed in Table 9.2 and the result of the simulation is shown on the measured characteristics in Fig. 9.6. With supplies of 5 volt and −3 volts, a workable logic inverter occurs. The logic threshold is −1 volt and a 1.7 peak-to-peak swing is correctly inverted.

The remaining test circuits on the first mask include a full adder circuit with separate inverter and output driver circuits for individual testing. Unfortunately the poor diode geometry prevents their function because the input and output logic levels are not compatible between adjacent gates.

**Second Mask**

As with the first mask, the capacitor coupled logic circuits were part of another project and were not tested. The sample-and-hold circuit (also part of another project) could not be tested because the long gate lines did not form properly.

The other circuits were not functional because of the etching problem with narrow devices described in section 9.1.6. There is a test structure with progressively narrower
devices but the widest of these was affected by the etch. It is believed that the designs will work once the fabrication difficulty can be eliminated.

Three BFL inverter circuits with 18, 36 and 72 μm switch transistors are included on each chip of the second mask. Despite the fabrication problems some of these devices were successfully tested. The simulation of these circuits was performed with various sets of parameters corresponding to the different effective pinch-off potential of the various device widths. Table 9.3 lists the calculated model parameters for the second mask as a function of pinch-off potential. The pinch-off potential appropriate to the device width was chosen on the basis of the results shown in Fig. 9.4.

### High Speed Measurement

The measurement of the high frequency performance of the inverter circuits on the second mask required high performance microwave equipment. Initially a Hewlett Packard HP 8510 network analyser with signal generator, a sampling oscilloscope and a Cascade Microtech microwave probe station was used. The use of high quality 18 GHz probe heads proved to be a significant advantage. The main problem with testing

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**Figure 9.7.** Schematic showing test set up for measuring inverters at high speed.
circuits at high frequency is that significant losses which are difficult to quantify occur in the cables and probe heads. Therefore the measured signal amplitudes included large error estimates (up to 1.2 dB).

The test set up is shown in Fig. 9.7 and the cable losses and signal level at the input to the circuit are listed for various frequencies. The cable losses were determined with the network analyser and included the probe contact to the wafer. The probe contact continuity was reproduceable within a 1 dB variation (12 %).

The measurements made on the medium size (36 μm) inverter in chip M-2(3)J are shown in Photos 9.8, 9.9 and 9.10 for inputs at 2.5, 4.5 and 5.5 GHz. The phase relation between the traces shown in the photos were aligned by probing a straight wire connection over a distance equal to the spacing between the input and output of the inverter under test. Therefore the phase difference between the input and output is created by the inverting action of the circuit. Operation of the inverter deteriorated rapidly beyond 5.5 GHz and the output amplitude dropped to a residual non-inverted signal.

Simulation of the measured inverter was carried out using the parameters listed in Table 9.3. Reasonable agreement with the measurement was achieved within an error of 1.2 dB (15 %). It is important to note that during the measurement a 50 Ω load is present at the output of the inverter and the output is attenuated by this loading. Fig. 9.8 shows the simulation at 2.5 GHz which corresponds to Photo 9.8.
Photo 9.9. Operation of medium size inverter on chip M-2(3)J at 4.5 GHz. The upper trace is the input signal and the lower is the output. An inverting action occurs but the gate delay is causing a phase shift.

Photo 9.10. Operation of medium size inverter on chip M-2(3)J at 5.5 GHz. The upper trace is the input signal and the lower is the output. The inverting action is being masked by the gate delay.
The transfer characteristic of the inverter was measured and the result is shown in Fig. 9.9. This cannot be correlated to the high-speed test with the 50 $\Omega$ loading.

What can be pointed out is the importance of using the correct pinch-off potential and parasitic resistance values for each device in the circuit. The circuit was designed using the procedure described in Chapter 5 with the assumption that each device is identical except for width. The expected dc transfer predicted by SPICE is shown as a broken line in Fig. 9.9. However, the fabrication process reduced the pinch-off potential of the narrow devices as shown in Fig 9.4 and the geometry of the ohmic contacts varies between devices. Accounting for these variations gives the solid line prediction in

**DC Measurements**

The transfer characteristic of the inverter was measured and the result is shown in Fig. 9.9. This cannot be correlated to the high-speed test with the 50 $\Omega$ loading.

What can be pointed out is the importance of using the correct pinch-off potential and parasitic resistance values for each device in the circuit. The circuit was designed using the procedure described in Chapter 5 with the assumption that each device is identical except for width. The expected dc transfer predicted by SPICE is shown as a broken line in Fig. 9.9. However, the fabrication process reduced the pinch-off potential of the narrow devices as shown in Fig 9.4 and the geometry of the ohmic contacts varies between devices. Accounting for these variations gives the solid line prediction in
Fig. 9.9. Each device in the inverter circuit shown in Fig. 9.10 is annotated with the drain and source resistance, pinch-off potential and width of each device. The pinch-off potential appropriate to the device width was chosen on the basis of the results shown in Fig. 9.4. These values and the other model parameters are listed in Table 9.3 and were used to produce the better match to measured data in Fig. 9.9.

**Voltage Contrast Microscopy**

The high-speed and dc measurements were repeated with a Voltage Contrast Microscope. This is basically an electron microscope adapted so that the intensity of the image is a function of the potential at the surface of the sample being viewed. An SEM picture of the inverter taken with the voltage contrast microscope is shown in Photo 9.11. (A corresponding schematic is shown in Fig 9.11.) The darker metal areas in the picture are at a more positive potential. The image can be focused on a small area of one of the metal connections and the ac variation monitored by the intensity of the image. Thus the voltage contrast microscope is a powerful minimally invasive probe.

The inverter was tested with a Cambridge Instruments Voltage Contrast Microscope and Telecom Research Laboratories in Melbourne. A 730±10 ps sampling gate is used and a computer interprets the image to build up an oscilloscope-style display of the potential at the image point. The accuracy of the reading is limited by electric fields from nearby bonding wires.
The measurements are shown in Chapter 7 Figs. 7.3 and 7.4 along with a SPICE simulation. The agreement with timing and dc levels is very good noting that the voltage contrast measurement of the positive potential part of the signal is exaggerated by the nearby +4 V bonding wire. A SPICE listing for the simulation is also given in Chapter 7.

Photo 9.11. Voltage contrast microscope view of an inverter. The darker metal is at a more positive potential.

Figure 9.11. Schematic of Photo 9.11.
Photo 9.12. Close-up of a four input AND-NOR-AND gate from the shift register circuit of the second mask set. There are three air-bridges carrying power supplies. The two dual gate switch transistors can be seen at the left of the image.

Photo 9.13. Close-up of a NAND-NOR gate from the shift register circuit of the second mask set. The bonding pads are 100 × 100 µm.
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Design and Performance of Locally Fabricated GaAs Digital ICs

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SUMMARY The University of Sydney, School of Electrical Engineering and the CSIRO Division of Radiophysics are collaborating to design and fabricate high-speed Gallium Arsenide digital integrated circuits. The first circuits are based on a depletion mode MESFET technology and will use high quality material grown by molecular beam epitaxy. Transistor gate widths are initially 2 micrometres with 1 micrometre spacing to allow use of local mask-making facilities. This paper outlines the technology being used, discusses circuit design techniques and constraints imposed by that technology, and gives performance estimates for fabricated circuits. The work is targeted primarily at communications applications.

1 Introduction

Gallium Arsenide is a key ‘enabling’ technology with superior speed-power product that permits the development of systems that have been impossible or impractical to construct using silicon semiconductors. As a result, GaAs ICs are found increasingly in very high performance systems in communications, computers and instrumentation (Oxley & Forrest, 1986)

High performance digital ICs will be especially important for switching and signal processing in future telecommunications systems such as the integrated broadband communications services planned for introduction in the next decade. These will require high speed trunks together with local area and subscriber networks capable of carrying video information to each subscriber. Digital GaAs ICs will be of primary importance in carrying out multiplex/demultiplex functions at the ends of these links and have potential application in equalisation of the links.

In order to encourage system designs in these areas in Australia, the Laboratory of Communication Science and Engineering at Sydney University and the CSIRO Division of Radiophysics are collaborating to establish a local GaAs digital integrated design and fabrication capability. To achieve this goal, we are focusing on the production of a high-speed digital filter. Construction of the filter requires development of the very high speed digital circuits achievable with GaAs technology.

This paper reports current work in this project. The paper is structured as follows. Section 2 describes the initial fabrication process used for developing a basic design capability. Section 3 reports on work undertaken for device modelling and simulation. Section 4 presents circuits for two logic families chosen as most suitable for the current fabrication process. Section 5 shows the layout of our first test die and discusses the development of a gigabit-rate functional chip tester for GaAs logic circuits. Section 6 reports on an educational programmes aimed at establishing a community of knowledgeable designers in time to capitalise on research programme achievements. Some areas of future investigation are noted in the conclusion.

2 Fabrication Process

The fabrication process uses a seven mask, mesa isolation technique and airbridges to achieve two levels of metalisation. Active devices are the Schottky barrier diode and the depletion mode MESFET.

The process begins with a doped wafer. Note that there are two distinct types of active layer growth which have different doping profiles. An implanted layer has an extended doping profile and needs deep mesa isolations. For example, a wafer with a nominal doping of $2 \times 10^{17} \text{ cm}^{-3}$ to a thickness of $0.47 \mu \text{m}$ typically tails off to around $10^{15} \text{ cm}^{-3}$ at $0.65 \mu \text{m}$ and semi-insulating material is not reached until $\approx 2 \mu \text{m}$. A doped layer with a sharp profile, such as one grown by molecular beam epitaxy (MBE), is preferred because it allows more shallow mesas.

To date work has been carried with third party wafers of both types but production at CSIRO of doped wafers using an MBE process has commenced recently.

The fabrication process proceeds with the following steps (see fig. 1):

1. The first mask defines the mesa structure. The mesa is formed with a process which gives gentle sloped faces in only one crystalline direction. Thus wiring is routed so that it crosses mesa boundaries in this direction. The depth of the mesa depends on the quality and type of substrate and must be deep enough so that the active layer is removed.

2. The second mask defines the Au/Ge/Ni ohmic metal and first level of wiring.

3. The third mask defines the gate and Schottky metal. The resist is exposed and then the gate regions are recessed to set the transistor pinch-off voltage. Schottky metal is applied after etching.

4. The fourth mask is an underdoped Ohmic mask used to lay gold over the ohmic metal to improve the electrical properties.

5. The fifth mask prepares for airbridge metal build-up and is used to cover the entire wafer with resist except where second level wiring is to contact the first level. Then a thin layer of Au is deposited over the entire surface.

6. The sixth mask defines the second level wiring which is built up by electroplating. The resist and first sheet of gold is removed to leave an airbridge structure.

7. The final mask is used for passivation.
A conservative set of design rules for circuit layout has been developed after careful consideration of lithography, alignment, processing and electrical design requirements. The limiting consideration is lithography which restricts the minimum gate size to 2μm but with gate-source, gate-drain and gate-gate spacing down to 1μm. Sub-micron gate lengths which call for electron beam lithography will soon be required to produce faster circuits.

3 Device Modelling

A fundamental requirement for any integrated circuit design is the ability to accurately simulate the circuit before manufacture. To this end, the development and verification of simulation models that closely match FET measured characteristics has been a major area of investigation.

A MESFET model has been developed and adapted for use with the existing SPICE 2G program. The model for drain current in an n-channel GaAs MESFET is described by the following equation (Curtice, 1980):

\[ I_d = \beta(V_{gs} - V_T)^3(1 + \alpha V_{ds}) \tan h(\alpha V_{ds}) \]

SPICE 2G doesn’t use the hyperbolic tangent function to describe saturation which renders it unsuitable for MESFET design. However, the tangent function can be approximated by using the exponential function which describes a reversed biased diode.

The application of the reverse biased diode in a MESFET model which can be used as a SPICE subcircuit is shown in figure 2. DTANH’s diode model parameters are set so that the reverse current approximately equals Tanh(Reverse Bias Voltage) with no Frequency or Temperature dependence. The voltage applied to this diode by ETANH is \( \alpha V_{ds} \).

The JFET is held in the saturated region by a 100V DC source and LAMBDA is set to zero so that the current through the 100V source is proportional to \( (V_{gs} - V_T)^3 \). The SPICE Parameters BETA and VTO are set to those of the MESFET and the gate junction capacitance is provided in the SPICE JFET model by setting the parameters CGS, FC and PB.

The current controlled current source FMESFET is a two dimensional nonlinear source proportional to the currents through the 100V source and VTANH. Thus this current is described by

\[ I = \beta(V_{gs} - V_T)^3\left[1 - \exp(-1.45\alpha V_{ds})\right] \]

This is a close approximation to the equation developed by Curtice with \( \lambda = 0 \).

The remaining elements are the contact resistances \( R_s \), \( R_t \) & \( R_d \) which cannot be set to zero (because of a limitation with SPICE) but can be omitted or set to an arbitrary small value. Additional fixed value stray capacitance can be included as required.

With this model, the circuit requirements and limitations of GaAs approaches have been studied and a procedure has been devised so that logic circuit designs, based on power and speed requirements, can be evaluated. Additionally, other simplified models for large scale simulations, and more detailed models for use as ‘benchmarks’ to test the validity of simplifying assumptions, are being studied.

The development of a benchmark model has involved the detailing of basic GaAs crystal, electrical and quantum mechanical properties. It has taken considerable effort to overcome the limitation of currently published models (e.g. Pucel et al., 1975) which are designed for specific applications and, as general models, do not fit measured data. This work is continuing with the development of a two dimensional numerical simulation model which solves Poisson’s potential and Boltzmann’s electron transport equations (Snowden, 1985). A simple simulation program has been developed which demonstrates the feasibility of this approach. The resulting model gives a detailed picture of device behaviour and is adaptable to future technological changes.

4 Logic Circuit Design

Different design approaches for GaAs logic circuits were compared with a view to choosing one most suited to the local fabrication facilities. A number of comparisons of different logic circuit approaches are available in the literature (Long et al., 1982; Eden, 1982; Nurillat et al., 1982). Two logic families - Buffered FET Logic (BFL) and Capacitor Coupled FET Logic (CCFL) - were selected for further investigation including detailed design, simulation and layout.

BFL circuits give high speed and high noise margins with good tolerance to process and temperature variations but use dual supplies and have relatively high power dissipation. Figure 3 shows a BFL NOR circuit. CCFL uses less area, requires only one supply and offers lower power dissipation at speeds comparable to BFL. However, a significant disadvantage is a minimum clock frequency which may cause testing difficulties. Two cascaded CCFL inverter circuits are shown in figure 4.

5 Test Chips

A 2mm x 2mm die incorporating test structures, simple logic gate layouts and a one-bit full adder layout has been prepared and is in the process of being fabricated. Both CCFL and BFL test circuits are included in the die. The layout of the die is shown in figure 5a, with legend in figure 5b. Masks were prepared using our Computervision CAD system and the AWA Electromask facility. Simulations for 2μm x 12μm gates predict performances close to 100 psec propagation delay for both BFL and CCFL gates.

Chip Test Hardware

Verification of the correct functional operation of gigabit rate digital circuits presents a special problem. Since it is expected that the adequacy of solutions to the problems of testing will significantly influence the application of GaAs technology, we have undertaken the development of a prototype gigabit-rate digital test system.

The requirement is for the development of equipment to stimulate and monitor digital signals at gigabit rates. The test system will be based on a custom GaAs chip designed at CS&E and currently being fabricated by a US foundry, Triquint Semiconductor Inc. This chip is a specialised, cascadable, 8-bit shift register which is capable of acting as both a driver and a monitor of digital GaAs circuits. The basic structure of the tester will follow the approach used for our earlier chip testers (Skellera et al., 1983).

Apart from the custom GaAs shift register chip, development of the tester will require special attention to packaging because the environment around the die may substantially effect test results. In particular, signal skew delays, the effect of crosstalk and microwave propagation effects must be considered.

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6 Educational Programme

The early introduction of courses is viewed as an important contribution which will establish a base of design engineers able to use GaAs technology. GaAs IC design courses were given in October, 1986 at the University of Sydney and in November, 1986 at the CSIRO. A course is also offered in the Master of Engineering Studies postgraduate teaching programme at the University in 1987. It is planned to incorporate material from this into an intensive industry-oriented course on GaAs integrated circuit design.

7 Conclusion

This collaborative establishment of an Australian GaAs digital integrated circuit technology requires not only the development of a broad range of technical expertise but also addresses the need to transfer these skills to industry. Thus, the project has three goals;

1. to develop the design, fabrication, packaging and testing techniques needed to produce custom Gallium Arsenide logic circuits;
2. to establish a GaAs logic circuit design facility with skills accessible to Australian industry;
3. to raise industry awareness of and skills in GaAs design through an educational programme involving specialist seminars and courses.

We will proceed to design and fabricate increasingly large digital circuits by devising architectures and integrated system design procedures suitable for GaAs technology. Additionally, we will continue investigations of new fabrication processes and design styles. Of special interest are:

- the fabrication of enhancement mode devices with molecular beam epitaxy. These are desirable in logic design because they enable a simpler logic gate operating from a single power supply and dissipate only a small fraction of the power required for depletion mode logic families. Large scale circuits will require enhancement mode devices.
- logic circuits based on HEMT structures, which can be fabricated only with an MBE process. HEMT (MODFET) circuits (Drummond, 1986) have the potential for higher speed at lower power than those based on the GaAs MESFET.

8 Acknowledgments

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9 References


Figure 1. Cross-section of a MESFET structure with an airbridge connection. Note that the process uses a mesa isolation and that device threshold potential is set by thinning the channel region.

Figure 2. SPICE subcircuit used to implement a MESFET model. The JFET is saturated by the 100V source so that the MESFET saturation can be simulated by the Tanh diode network.

Figure 3. A Buffered FET Logic (BFL) NOR gate. This family runs with two power supplies at about 10mW/gate. NAND and NOR logic can be used with high fan out and low sensitivity to process variation but occupies a large area.

Figure 4. Capacitor Coupled FET Logic (CCFL). This family features single power supply operation at about 0.1mW/gate and occupies relatively small area. However, the circuit must operate at high frequency and has a low fan out capability.

Figure 5a. Detail layout of the test structure die currently being fabricated.

Figure 5b. Legend to die layout. The 2mm x 2mm area incorporates test structures designed to check the operation and limitations of the fabrication process.
Development of GaAs Device Models for Digital Circuits

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Sydney University’s School of Electrical Engineering, in collaboration with the CSIRO Division of Radiophysics, is developing GaAs digital integrated circuit technology. Simulation for this programme has been approached from a fundamental level so as to develop Schottky diode and MESFET models for the existing SPICE programme. The derivation of model parameters for his purpose has required the detailing of basic GaAs electrical properties. This paper describes these models and how the parameters were derived.

1 Introduction

The GaAs Metal Semiconductor FET (MESFET) is suited to high speed digital circuits with typical delays of 100-ps/gate [Eden 1982]. Sydney University’s School of Electrical Engineering, in collaboration with the CSIRO Division of Radiophysics is developing GaAs technology so that the superior speed-power product of these devices can be exploited [Skellern et al. 1987].

To date, the work has concentrated on the requirement to accurately model Schottky barrier diodes and MESFETs. The approach has been to study the electrical properties and physical details of the devices and derive parameters required for adapting existing SPICE models. This paper outlines the use of these models and the theory behind the model parameter selection.

2 Simulation and Modelling

The extent of the simulation depends on the scope and complexity of the circuit. An elemental gate should be accurately modeled to give reliable figures of merit such as gate delay and fan-out. For more complex logic circuits it is necessary to use faster techniques such as switched resistor capacitance models using parameters derived from the detailed simulations. Although simple models are used for large circuits, it is essential to have a detailed model to test the validity of the simplifications.

The existing SPICE computer programme is suitable for gate level modelling. However, it is necessary to have elemental equivalents for resistances, capacitances and the main active devices including the Schottky diode and MESFET. The determination of parameters begins with the basic GaAs electrical properties.

2.1 GaAs Electrical Properties

The electrical and transport properties including mobility are characteristics that favour GaAs devices for high speed work and distinguish them from silicon devices. In order to understand the devices, limitations and modelling of GaAs circuits, these properties should be well defined.

The GaAs crystal forms a brittle wafer with a low thermal conductivity. There is a wide band gap with low intrinsic carrier concentration which gives a high resistivity semi-insulating substrate (6.9x10^16 Ω.cm). The important properties, including electron mobility, of GaAs at 300 K are listed in table 1 [Sze 1969].

<table>
<thead>
<tr>
<th>Property</th>
<th>Value (at 300K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility (cm²/Vs)</td>
<td>8500</td>
</tr>
<tr>
<td>Hole Mobility (cm²/Vs)</td>
<td>400</td>
</tr>
<tr>
<td>Specific Heat (J/g°C)</td>
<td>0.35</td>
</tr>
<tr>
<td>Thermal Conductivity (W/m°C)</td>
<td>0.46</td>
</tr>
<tr>
<td>Work Function (eV)</td>
<td>4.7</td>
</tr>
</tbody>
</table>

The electron drift velocity, in GaAs at low electric field, is proportional to electric field strength and decreases with higher impurity concentration because of scattering effects. An empirical relation for low field mobility is \( \mu_e = 1.94 \times 10^6 N_d^{0.15} \text{cm}^2/\text{V}s \), where \( N_d \) is doping concentration [cm⁻³]. This a good fit to experimental data [Hilsen and Rose-Innes 1961] for doping concentrations between 10¹⁵ and 10¹⁹ cm⁻³.

where \( \mu_e \) is the high field saturation velocity. Maximum velocity is maintained at a domain sustaining field, \( E_s \), which is approximately the same as the characteristic field, \( E_c = 3.200 \text{ V/cm} \).

3 Planar Ohmic Contacts

The structure of wiring on a planar device necessitates the use of adjacent contacts which do not have uniform current density over their total area. The contacts consist of a metal to GaAs interface with a contact resistance, \( r_c \) per unit area in the vertical direction. The GaAs material under the contact has a sheet resistance, \( r_s \) per square in the horizontal direction. If the contacts are separated by a distance \( 2d \), the sheet resistance of the GaAs between them
is $r_2$, $d$ per unit width. However, the effective distance between the contacts will be greater than this because of the finite contact resistance. By defining a transfer length, $L_d$, for each contact [Marlow and Das 1982], the separation becomes $2d+2L_d$ and the sheet resistance becomes $r_s(2d+2L_d)$. The transfer length is the effective length of the contact so that the contact resistance can be equated with the sheet resistance under it. Thus $r_sL_d = \frac{r_s}{2}$. 

An epitaxial layer of GaAs material with depth $d$ and doping $N_d$, has resistance $r_s = \frac{1}{q\mu N_d}$ so if $r_s$ is known, the combined resistance for unit width of a contact and epitaxial layer extending a distance, $d$, is given by 

$$r = \frac{d}{\mu N_d} \sqrt{\frac{25e}{80N_d}}$$

4 Inter-electrode Capacitance

With a set of capacitance equations, proposed by van Tuyl [1980], it is possible to calculate parasitic elements to include in the models. The method gives the coplanar capacitance in Farads per microm, $C_e$, between two conductors with length, $l$, separated by a distance, $d$, and the capacitance of each element to ground.

$$C_e = \frac{1.39 \times 10^{-17} (\varepsilon_r + 1)}{ln(4(l+d))} \quad 1/d \leq 0.75$$

$$C_e = \frac{2.82 \times 10^{-18} (\varepsilon_r + 1) ln(4(l+2d))}{ln(4(l+d))} \quad 1/d > 0.75$$

The capacitance to ground is given by

$$C_{gr} = 5.56 \times 10^{-17} \left[ \frac{z \varepsilon^*(w)}{ln(8h/w)} + \frac{w \varepsilon^*(z)}{ln(8h/z)} \right] - 8.85 \times 10^{-18} \frac{\varepsilon_r w z}{h}$$

where $\varepsilon^*(x) = \frac{\varepsilon_r + 1}{2} \frac{\varepsilon_r - 1}{\sqrt{1 + 12(h/x)}}$, $z$ and $w$ are the conductor's width and length and $h$ is the height above ground.

The combined ground and coplanar capacitance is

$$C_t = \frac{C_{gr}^2 + C_e^2}{C_{gr} + C_e}$$

With these equations it is possible to calculate the parasitic elements to include in the models.

5 SPICE Schottky Diode Model Parameters

When supplied with appropriate parameters, the diode model contained in SPICE 2G becomes suitable for simulation of GaAs Schottky junctions.

5.1 SPICE Diode Model

The basic equation for diode current adopted by the SPICE DC model is

$$ID = IS \left( \frac{V}{V_{FN} - 1} \right) + V \cdot G_{min}$$

where $IS$ is the reverse leakage current and $V$ is the forward potential applied to the junction. $G_{min}$ is the minimum conductance allowed by the program (used to ensure convergence) with default value $10^{-12}$mhos. A parasitic series resistance, $RS$, is also included.

As mentioned above, the forward characteristic of a real diode can be modeled using the experimental data (as shown in Figure 5.1) to create a SPICE model. The relationship between the current and voltage is

$$V = I / R_S + (1 + R_S / R_D) \cdot V_{FB}$$

where $R_S$ is the series resistance, $R_D$ is the diode resistance, and $V_{FB}$ is the forward voltage. This model can be implemented in SPICE using the following equations:

$$V = \frac{I}{R_S} + \frac{R_S}{R_D} \cdot V_{FB}$$

The model includes junction capacitance $C_J$ and diffusion capacitance $C_D$.

$$C_J = \left( \frac{C_{JT}}{1 + \frac{V}{V_{FB}}} \right) \cdot C_{JT}$$

$$C_D = \left( \frac{C_{DD}}{1 + \frac{V}{V_{FB}}} \right) \cdot C_{DD}$$

The constants are identified below.

AC temperature dependence is modelled in terms of an empirical equation for the energy gap in silicon and is not suitable for GaAs applications.

The parameters IS, $N$, RS and $C_{JT}$ can be determined by examining the theory of operation of the devices with reference to the SPICE mathematical model.

5.2 Diode Model Parameters

The flow of electrons from the metal to the semiconductor through a Schottky junction is affected by the barrier imposed by the difference in work functions of the two materials. The height and shape of the barrier can be defined as follows:

$$\phi_B$$ position of maximum barrier height at $x_m$

$$\Delta \phi$$ amount by which the barrier has been lowered by the Schottky effect

$$V$$ external bias imposed at $x=W$

At the surface of GaAs, the existence of extra energy states in the energy gap reduces the width of the gap. The resulting effect on the barrier height is given by $\phi_B = c_1 \phi_m + c_2 - \Delta \phi$ where $\phi_m$ is the work function of the metal. If $c_1 \to 0$ the Fermi level is tied to that of the surface states. This occurs when there is a high density of surface states and they can be filled in preference to transferring charge to the metal. On the other hand if $c_1 \to 1$ then the barrier is not affected by surface states and is simply the difference in the work functions. Measured data [Sze 1969] for GaAs gives $c_1 = 0.07 \pm 0.05$, $c_2 = 0.49 \pm 0.24$ V. So for an Al gate $\phi_B = 0.73$ eV.

The barrier is also affected by the doping level which varies the number of conduction electrons near the contact. An empirical formula [Fukui 1979] for aluminium is $\phi_B = 0.026 x \ln(N_d) - 0.25$ [volts] where $N_d$ is the doping concentration in carriers per cm$^3$.

5.2.1 Reverse Saturation Current and Emission Coefficients

The parameters IS and $N$ can be found by considering thermionic Emission-Diffusion Theory [Sze 1969]. For an electron moving into the semiconductor the barrier is a potential well formed by the positive charge left on the material surface and the imposed electric field $E$. The barrier maximum occurs at a distance $x_m = \frac{3}{16 \alpha} E$ from the contact, and is lowered by

$$\Delta \phi = 2E x_m$$

in a uniform field $E$.

Consider first, the flow of electrons between the contact and $x=x_m$ with the condition that $x_m$ is close enough to the barrier so that there are no optical-phonon scattering effects but not short enough for tunneling or breakdown (9kV/cm < $E < 100kV/cm$). To achieve this condition in a practical diode, a reverse bias is required and the flow of electrons from the semiconductor to the metal will be negligible. Assuming a Maxwellian velocity
distribution and a barrier height many times q/kT above the Fermi level, the current density of electrons moving from the metal to the semiconductor is given by the Richardson-Dushman equation [Jay 1984]. This current is the reverse leakage current which in the SPICE notation is

\[ IS = A_m T_{nom}^2 \frac{A_{sym}}{2} \exp \left( \frac{-q \phi_m}{kT} \right) \text{ per unit area.} \]

The Richardson constant, \( A = 1.2 \times 10^6 \text{ A/m}^2/\text{K}^2 \) is adjusted for the effective mass in the metal so that \( A_{sym} = A \frac{m}{m_{m}} \).

Once the electrons arrive in the semiconductor, they may be slowed down by interaction with it. Thus the equation is valid only if the emission velocity, \( v_R = \frac{A_{sym}^2}{qN_C} \approx 10^6 \text{ cm/s} \) [Sze 1969], is smaller than the drift velocity, \( v_D = \mu E \), in the semiconductor. This condition is satisfied with reverse bias and the Richardson equation is valid.

When \( x_m \) becomes large enough, scattering occurs before the barrier is reached. The velocity in the forward direction is limited by drift in the region between \( x_m \) and \( W \) and at high bias, the current is limited by the effective resistance of this region.

At a neutral bias electrons are thermally emitted into the metal with a current density equivalent to \( ID = A^* T^2 \frac{n}{N_C} \), which is the Richardson-Dushman equation at zero potential, \( V = \phi_B \), with a weighting for the number of filled conduction states. \( A^* \) is adjusted for the semiconductor.

The SPICE emission coefficient, \( N \), can be evaluated by fitting the SPICE equation to the points \( V = \phi_B \), \( ID = A^* T^2 \frac{n}{N_C} \), and \( V = \infty \), \( ID = IS \). Thus

\[ N = \frac{q \phi_B (V = \phi_B)}{kT} \left[ \ln \left( \frac{A^* \frac{n}{N_C} \exp \left( \frac{q \phi_B (V = \infty)}{kT} \right)}{A_{sym}^2} \right) + 1 \right] \]

DC temperature dependence parameters are the activation energy, \( E_G \), and the saturation-current temperature exponent, \( X_T \), which should be set to \( N \phi_B \) ad 2N respectively.

At high reverse bias the junction will break down either by avalanche or, if \( x_m \) is small enough, by tunneling. A formula for abrupt junction avalanche breakdown voltage is given by \( 2.81 \times 10^{18} N_C^{3/4} \) [Sze 1969]. The SPICE parameters IBV and BV can be set appropriately.

5.3 Resistance

In planar devices, a significant resistive component arises at forward bias because the current through the Schottky junction is concentrated on the edge closest to the ohmic contact.

The forward biased diode contact gives a voltage drop associated with an equivalent small area signal contact resistance \( r_c = \frac{A_n K T}{q} \ln \left( \frac{1}{A_{sym}} \right) \Omega \text{-m}^2 \) where \( A \) is the effective area of the contact. The transfer length for the diode contact becomes \( L_d = \frac{A_{sym}}{2} \left( \frac{1}{z} \right) \) where \( z \) is the contact width. Substituting for \( R_d \) and squaring gives, to a first degree approximation,

\[ \frac{A_{sym}}{2} = \left( \frac{1}{z} \right)^{1} + \left( \frac{1}{z} \right)^{1} \]

The value of \( A \) is constrained by the physical dimensions of the contact and is a decreasing function of current.

The ideal contact has a constant transfer length equal to its length, \( L_d \), but in reality is reduced so as to increase the potential drop. The effective resistance is obtained by dividing this potential increase by the current through the diode. Adding the ohmic contact resistance gives a total series resistance of

\[ R_S = \frac{N C T}{I_d} \ln \left( \frac{1}{1 \text{-} \ln \left( \frac{q \phi_B}{kT} \right)} \right) + \frac{1}{a} \frac{1}{1 \text{-} \ln \left( \frac{q \phi_B}{kT} \right)} \frac{1}{\text{au} N_d} \]

5.4 Capacitance

The usual expression for junction capacitance, derived with Gauss’ law, is \( \frac{C_J}{C_T} = \frac{2(q \phi_B V)}{q \epsilon_C N_d} \). The applicable parameters are the zero bias junction capacitance, \( C_J = \sqrt{\frac{q \epsilon_N}{2 \pi \epsilon_B}} \) and the junction potential, \( V_J = \phi_B \). The grading coefficient, \( M \), and Capacitance coefficient, \( F_C \), can be left at their default values of 0.5. Geometry effects such as saturation as the bottom of the epitaxial layer is encountered [Takahara 1982] are not modeled in SPICE.

At high fields minority carrier (hole) injection occurs with a minority carrier storage time, \( t_s \), typically less than \( 10^{-15} \text{s} \) in GaAs. This is negligibly small so that the SPICE parameter TT can be left at the default zero value.

6 MESFET Models for SPICE

6.1 SPICE MFSFET Model [Quarles 1986]

SPICE version 3A7 MESFET model is a cubic approximation of the empirical model developed by Curtice [1980], which describes drain current saturation by a hyperbolic tangent function. The drain current equation is

\[ I_{ds} = \frac{B(V_G - V_T)^2}{1 + B(V_G - V_D)} \tan h(\alpha V_{ds}) (1 + A V_{ds}) \]

where \( B \) is a dopant tail extending parameter, \( V_{T0} \) is the threshold bias for channel cutoff and \( \beta \) and \( \alpha \) characterize the MFSFET. Note that the current saturation occurs at constant source drain potential independent of the gate bias. The gate diode junction and capacitance is modeled between the drain and source by two SPICE diode elements.

6.2 Adaptation of the JFET model to GaAs

To implement a MFSFET with earlier versions of SPICE, it is necessary to construct a lumped element subcircuit based on the JFET model.

The tangent function, used by Curtice, can be generated by using the current flowing through two back-to-back diodes in the subcircuit opposite.

The diodes DTANH1 and DTANH2 have model parameters chosen so that the current through them and source VTANH is \( \tan h(10 \times \text{Bias Voltage}) \mu A \). The voltage applied to this diode by ETANH is set to \( \frac{10}{10 V_{DS}} \)

The JFET is held in the saturated region by a 100V source so that the current through the source is proportional to \( (V_G - V_T)^2 \). The current controlled source function FMESFET is a two dimensional nonlinear source proportional to the currents through the 100V source and VTANH. Thus this current is \( I \propto (V_G - V_T)^2 \tan h(10 \times \text{Bias Voltage}) \mu A \) as required.
Discrete diode elements, to simulate the gate junction, and parasitic elements are added as required. The gate-source and gate-drain junction capacitance is a result of reverse biased Schottky junctions which are modeled by SPICE diode elements. The gate dimensions are divided between the source and drain and are used to determine the appropriate model parameters.

An alternative approach used by TriQuint Semiconductor [Rosario 1986] is to adjust the saturation voltage with a voltage controlled voltage source to reduce the gate-source potential of the MESFET before applying it to a JFET element.

6.3 Transconductance and Voltage Saturation Parameters

The FET model developed in Pucel's paper [1975] is based on the assumption that drain current saturation is a result of carrier velocity saturation. This divides the channel into two sections, region I close to the source where the carriers are accelerating and the field increases almost linearly towards the drain, and region II at the drain end where carriers have a constant saturated velocity.

At the source end of the channel the proportion of depleted channel is given by \( s = \sqrt{\frac{qN_{av} \Phi}{W_{00}}} \) where \( W_{00} = W_{00} + \Phi_{B} = \frac{qN_{av} \Phi}{2 \sqrt{E_{0}}} \) is the potential required to deplete the whole channel.

At the point along the channel where domain sustained velocity saturation occurs, the potential to the gate is \( V_{p} \) and ratio of depleted to active channel is \( p = \sqrt{\frac{V_{gs} - \Phi_{B} - V_{p}}{W_{00}}} \). The saturated current per unit width of gate is \( I_{m} = qN_{av} \Phi_{B}(1-p) \) where \( a \) is the Region I is a FET channel of length \( L_{1} \) with a drain potential \( V_{D} \). The current per unit width is \( I_{d} = \frac{a}{L_{1}} \rho_{n} (1-p) \) where \( f(s,p) \) is \( p = \rho_{n} \sqrt{\frac{2}{3}} (p^{3} - 3) \), [van der Ziel 1976]. Equating \( I_{m} \) and \( I_{d} \) gives

\[
L_{1} = \frac{L_{s} (p,s)}{\xi (1-p)} \quad \text{where} \quad \xi = \frac{E_{0} L_{s}}{W_{00}}.
\]

When saturation occurs \( L_{1} \) will be less than the actual channel length \( L \) and the remainder of the channel constitutes region II. Solving Laplace's equation in region II and including the voltage drop across region I gives the drain-source potential \( V_{ds} = W_{00} \left[ (p^{2} - s^{2}) + \frac{2a}{L_{s}} \sinh^{-1} \left( \frac{pL_{s} - L_{1}}{2a} \right) \right] \).

This equation in conjunction with the above expression for \( L_{1} \) can be used to solve for \( p \). Then given \( V_{sd} \) and \( V_{gs} \), \( I_{ds} = I_{m} \) can be found.

Before saturation \( V_{p} = V_{sd} \), \( L_{1} = L \) and \( \xi = \frac{E_{0}}{W_{00}} \) and so \( E \) can be found. At the onset of saturation \( V_{D} = \frac{1}{2} (\mu_{n} E_{0} V_{gs} + V_{D}) \) because \( E = E_{0} \). Thus \( V_{ds} = \frac{E_{0} L_{s}}{2} \left[ 1 - \frac{1}{4} \left( \frac{p^{2} - s^{2}}{3p^{2} - 3} \right) \right] \) which is empirically equivalent to \( W_{00} - \frac{E_{0} L_{s}}{2} \) at \( V_{gs} = 0 \).

This model can be used to determine the SPICE MESFET model parameters by matching the zero bias saturation current and the drain resistance at zero drain voltage in both models.

Equating the zero bias saturation current predicted by the SPICE MESFET to that predicted by Pucel gives \( I_{ds} = \beta V_{g} = I_{m} \). Substituting for \( I_{m} \) at \( V_{gs} = 0 \) and setting \( V_{p} = V_{ds} \) gives a final expression per unit width of \( \beta = \frac{A q N_{av} \rho_{n} E_{0} V_{gs} + V_{g}}{2E_{0}} \left[ 1 - \sqrt{\frac{E_{0}}{\Phi_{B} + V_{g}} + \frac{E_{0} L_{s}}{\Phi_{B} + V_{g} + E_{0} L_{s}}} \right] \)

The zero biased low-voltage resistance of the channel can be determined by considering the active region as a resistor with depth \( a(1-s) \) and length \( L \). Equating this resistance with that of the SPICE model gives an expression from which \( \alpha \) is obtained

\[
\frac{dR}{dV} = \alpha \beta V_{g}^{2} = \mu_{n} N_{av} \frac{4E_{0}}{L} \left( 1 - \sqrt{\frac{E_{0}}{\Phi_{B} + V_{g}}} \right)
\]

7 Conclusion

The study of GaAs electrical properties and devices facilitates the development of simulation models necessary for integrated circuit technology. It is possible to use the existing SPICE programme by building up subcircuits with appropriate parameters as outlined in this paper. This can form the basis for GaAs device characterization and modelling.

8 Acknowledgements

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9 References


Gallium Arsenide Integrated Circuits

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Gallium Arsenide (GaAs) is a key ‘enabling’ technology with superior speed-power product that permits the development of systems that have been impossible or impractical to construct using silicon semiconductors. As a result, GaAs integrated circuits are found increasingly in very high performance systems in communications, computers and instrumentation.

High performance digital integrated circuits will be especially important for switching and signal processing in future telecommunications systems such as the integrated broadband communications services planned for introduction in the next decade. These will require high speed trunks together with local area and subscriber networks capable of carrying video information to each subscriber. Digital GaAs integrated circuits will be of primary importance in carrying out necessary functions in the links.

In order to encourage system designs in these areas in Australia, the Laboratory for Communication Science and Engineering at the University of Sydney and the CSIRO Division of Radiophysics are collaborating to establish a local GaAs digital integrated design and fabrication capability.

Gallium Arsenide Technology

The interest in GaAs circuits over silicon has increased since the investigation of GaAs transistors in the early 1970s. The advantages are numerous and varied. For microwave analog work GaAs offers lower noise and power consumption than silicon. For military and space applications, GaAs integrated circuits offer exceptional radiation hardness. For automotive or geological applications, GaAs can work in wide temperature ranges between -200°C and +200°C and with improved fabrication up to 400°C. GaAs optical devices offer high speed sources and detectors for optical fibre networks.

Over the past decade, GaAs devices have displayed unequaled gain, noise performance, and bandwidth in analog microwave applications. Despite the very small sub-micron dimensions, manufacture in large quantities can be readily achieved. More recently, high speed digital circuits have been developed because of the high switching capability of GaAs devices. Typically, GaAs ring oscillator propagation delays are as low as 30 ps and logic switch time of less than 100 ps are ten times faster than their silicon counterpart.

The development of high speed logic gates with modest power dissipation and high density has increased interest in further refinement towards large scale and even very large scale integration (VLSI). This will allow the development of high speed signal processors, computer circuits and memory circuits. It would also be possible to integrate circuits with both the necessary speed and optical properties for intelligent optical fibre links.

The Australian Context

There is much international interest in GaAs circuits which has resulted in a competitive, though not fully developed, industry. The challenge in Australia is to find new areas of application so that a firm hold in the world market can be established.

New areas of development lie in the field of information technology and low noise microwave applications. One device which shows promise in these areas is the High Electron Mobility Transistor (HEMT) which offers higher speed and better noise performance than the conventional GaAs transistor.

The development of the HEMT requires a technique which produces an accurately layered crystal wafer by a Molecular Beam Epitaxy (MBE) process. This limits the type of circuit fabrication to a mesa isolation process where the active devices are separated on the wafer by etching away the regions between them thus leaving a mesa.

For digital circuits, the density of the circuit is limited by the mesa structure which occupies more area than the planar technologies used by overseas foundries. However, the development of a digital technology using this fabrication technique would allow the integration of analog and digital circuits on the one chip. This ability would overcome the speed limitation imposed when trying to get information on and off the chip.

There is a wide range of applications in the communications field which require both analog and digital processing. For example, a digital filter for satellite links requires analog to digital conversion before the signal can be processed. Another example is optical links which require analog handling of the optical information before the digital processing.

Thus there is a niche in the market which can be filled by an Australian GaAs facility. In addition, there are new areas for continued research which are presently in an infant state. For example, the development of an enhancement mode device would offer much improved integration capability when combined with the present depletion mode technology.
How we are taking up the Challenge

The Laboratory for Communication Science and Engineering at the University of Sydney and the CSIRO Division of Radiophysics are collaborating to establish a local GaAs digital integrated design and fabrication capability. To achieve this goal, we are focussing on the production of a high-speed digital filter for use in the demodulation circuit of a satellite receiver. At present, such a filter cannot be implemented with commercial integrated circuit technologies as data rates are too high (120 Mbit/s/sec). The challenge is to implement the design by developing the high speed potential of Gallium Arsenide digital integrated circuit technology.

The present state-of-the-art in GaAs digital circuits is larger and more power hungry than their silicon equivalents. However, the speed advantage outweighs the disadvantages. The challenges faced in the development include adapting to a new fabrication technique which impose limitations on the type of circuit that can be made and developing computer tools which enable rapid design and verification.

The work is at the stage where the building blocks for the implementation of the digital filter can now be produced.

Fabrication Capability

The Division of Radiophysics has a GaAs laboratory for developing microwave devices including the HEMT and are also able to fabricate digital integrated circuits. The fabrication process uses the mesa isolation technique and airbridges to achieve cross overs between two levels of wiring. Active devices available are the Schottky barrier diode and the depletion mode Metal Semiconductor Field Effect Transistor (MESFET) and the HEMT.

Development of a Design Facility

At the University of Sydney, a conservative set of design rules for circuit layout has been developed after careful consideration of lithography, alignment, processing and electrical design requirements. The limiting consideration is lithography which restricts the minimum feature size to 1.5 microns. Sub-micron features which call for electron beam lithography will be available soon and allow the production of even faster circuits.

In addition, fundamental work has concentrated on the requirement to accurately model Schottky barrier diodes and MESFETs with computer tools. The study of the electrical properties and physical details of the devices has led to the development of a new and detailed model which has been added to the existing silicon based circuit simulator. It has taken considerable effort to overcome the limitations of recently proposed models, which were designed for specific applications, and generally do not fit our measured data.

The fabrication process being developed in Australia by the CSIRO is being used as the basis for developing design procedures and circuit layout rules. The approach is oriented towards easy adaptation as process techniques improve. A set of basic logic circuits have been developed so that complex circuits can be fabricated by combining these in a rapid systematic manner. This is the forerunner to the establishment of a GaAs logic circuit design facility tailored to the anticipated local capability.

Our research is continuing with the study and development of the HEMT. It is also planned that research into the development of enhancement mode technology as well as applications such as intelligent data links and signal processors will be established.

Educational Programme

The early introduction of educational courses at the University of Sydney is viewed as an important contribution which will establish a base of design engineers able to use GaAs technology. GaAs integrated circuit design courses have been run and further courses, including an intensive industry-oriented course, are being planned.

Conclusion

This collaborative establishment of an Australian GaAs digital integrated circuit technology addresses not only the development of a broad range of technical expertise but also the need to transfer these skills to industry. Thus the establishment of the GaAs capability has three goals;

1. to develop the design, fabrication, packaging and testing techniques needed to produce custom GaAs logic circuits;
2. to establish a GaAs logic circuit design facility with skills accessible to a competitive Australian industry;
3. to raise industry awareness of, and skills in, GaAs design through an educational programme involving specialist seminars and courses.

Already the building blocks for the design and development of communication equipment such as a digital filter are available. In addition, even more ambitious projects and research programmes have been commenced. This is an exciting time for this field in which we will see the growth of a new and competitive industry in Australia in the very near future.
High Performance GaAs Operational Amplifier Design

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This paper presents the design of a GaAs Operational Amplifier. Detailed simulation of the design shows improved gain and frequency performance over reported GaAs Op-Amps. The circuit is suitable for large scale, high speed integrated Analogue/Digital system applications.

1 INTRODUCTION

The operational amplifier is a fundamental element of many analogue circuits including ADCs, DACs, switched capacitor filters, phase locked loops, integrators and differentiators. High speed versions of these building blocks will be essential in switching and signal processing for future telecommunications systems. Thus there is a need for a high speed operational amplifier.

This paper presents a GaAs operational amplifier suitable for integration with digital circuits. It therefore allows the designer to reduce the number of off-chip interconnections in a mixed digital/analogue processing system.

The achievement of a high open loop gain with wide bandwidth to approximate ideal operational amplifier characteristics is the prime objective of the design. The design gives a simulated open loop gain of 75dB and 2.5GHz gain bandwidth product. This represents an improvement on currently reported designs [1, 2 and 3].

2 TECHNOLOGY AND PROCESS CONSTRAINTS

The op-amp is designed to conform to a GaAs fabrication process developed at the CSIRO Division of Radiophysics. This process is characterised by a one micron depletion mode MESFET produced using an MBE process, an ability to fabricate schottky diodes and a limited range of resistor and capacitor values. The process uses mesa structures to isolate active devices and a second-level airbridge metallisation.

There appears to be little published on op-amps designed entirely with Silicon JFETs that could be used as a guide for designing a GaAs MESFET opamp. Circuit techniques employed in nMOS which don't rely on the insulated gate of devices [4] can be useful as a guide for GaAs designs. Like nMOS circuits GaAs suffers from low gain per stage and similar techniques can be applied to overcome this [1]. Level shifting techniques must also be modified to eliminate the need for enhancement mode devices.

The design process requires accurate device models. Recently a computationally efficient model has been developed at the University of Sydney and installed in SPICE version 3 [5, 6]. This models dc and ac characteristics of GaAs devices with parameters derived from the material properties, process parameters and device dimensions. The model was used in the simulations to check the design and determine the op-amp performance.

3 CIRCUIT DESIGN

The circuit design follows a typical three stage architecture: differential input stage to minimise common mode gain; single ended high gain second stage; output buffer. The op-amp is stability compensated for unity gain operation using phase lead compensation techniques. This provides an adequate phase margin. A minimum gate width of 20 µm is used in the op-amp.

The achievement of a high open loop gain with wide bandwidth involves some trade-off. Notable concessions are the limited output drive capability, a fixed supply voltage and hence fixed output swing levels. A more fundamental trade-off, however, is the need to balance gain against dc bias stability. Many high gain topologies prove to be extremely sensitive to minor process variations. This results in large shifts in the bias point, to the extent that circuit devices fall out of saturation or become cut-off.
3.1 Differential Input Stage

A differential stage is used at the input. This has low distortion, rejects common mode signals, can be biased to prevent saturation and, ideally, provide zero offset voltage.

The design shown in Fig.3.1a is a typical differential pair configuration using transistor loads. The gain is found, by simulation, to be approximately 7. One of the factors which restricts the gain is the output resistance of the transistors.

To improve the gain, the techniques of bootstrapping and cascoding are available (using both together is not practical because bias circuitry is complicated). However, neither appear in the final circuit because of the undesirable properties they introduce in the differential pair. Bootstrapping results in differences in the positive and negative going gains and restricts the output swing. Cascoding restricts an already limited common mode range.

An alternative method for improving gain is a technique proposed by Larson et al. [3]. It involves tying the gates of both load transistors to the output as shown in Fig 3.1b. This introduces positive feedback in the loop, increasing gain. If the gate of Q1 is driven high then the output voltage rises. As a result the gate-source voltage of Q3 rises and the current through Q1 and Q3 increases. Since the circuit draws a constant current through the current source of Q5 and Q6 the current in Q4 falls and the output voltage rises further. Bootstrapping of the common current source (the drain-source voltage of Q5 is fed back to the gate-source voltage of Q6) is also used to increase the drain-source resistance. Bootstrapping increases the resistance of the current source.

A disadvantage of the bootstrap arrangement is that the two transistors of the pair must have different pinch-off voltages, requiring an extra processing step. Simulation indicates an improvement in gain from 7 to over 150, with an output swing of ±0.1V.

3.2 Gain Stage

The gain stage has several functions. Its primary role is to add to the overall gain. The performance of this stage will determine the slew rate and output signal swing of the op-amp.

The circuit used for this stage is shown in Fig.3.2. In essence it is a bootstrapped load with a cascode driving stage. The cascode stage has been modified to improve biasing with a technique used by Scheinberg [1]. Strictly speaking it is no longer a cascode stage since the signal is applied to both input FETs. It does, nevertheless, increase the effective drain-source resistance of the FET’s and hence increases gain. The price paid for improved stability is that the circuit no longer avoids the Miller effect capacitance, unlike a standard cascode amplifier. This limits the bandwidth of the circuit.

The diodes connected to the input are part of the level shifting stage. Diodes are also necessary to raise the bias voltage at the source of Q1 so that a negative gate bias is maintained on Q1 and Q2. Large currents will flow if the forward bias on the Schottky junction gate of a MESFET exceeds about 0.4V.

Fine tuning of the bias point, to produce maximum signal swing, is achieved by adjusting the width of Q4. SPICE simulation indicates a gain of nearly 700, with a signal swing of ±1.7V (this is fixed by the need to operate all MESFETs in saturated mode). The overall gain of the two stages is 100dB, substantially greater than the accepted minimum gain required for an op-amp of 60dB [1].

3.3 Output Stage and Interstage Level Shifting

The level shifting and output buffer stages both consist of unity gain source followers. They buffer the incoming signal against load current requirements and also provide dc level shifting. The two stages are shown in the complete op-amp circuit shown in Fig. 3.3. They operate as source followers with unity gain.

3.3.1 Interstage Level Shifting

To avoid enhancement mode devices, level shifting in GaAs is provided by diode chains. A
disadvantage of diode level shifters is that they limit the allowable supply voltage levels of the op-amp. (Note that an alternative technique to avoid this is proposed by Scheinberg [1]).

The current drive requirement of the interstage level shifter is small as it only drives two gates at the input to the second gain stage, hence it is constructed from minimum size gate widths.

3.3.2 Output Stage

The characteristics of the output stage determine the current drive capability of the op-amp and contribute to the output resistance. In contrast to the interstage level shifting circuit the output stage must provide high current drive capability since even when driving 'on chip' loads it may be required to drive many gates. It therefore has larger gates to provide this drive capability.

3.4 Compensation

The process of compensating the MESFET op-amp proved a difficult task due to the existence of two significant poles. Signal feedthrough effects and a non-minimum phase system response, with its characteristic large phase shift, prevented the successful implementation of pole splitting compensation. Suitable compensation is achieved using a lead compensation network. To ensure stability the op-amp is compensated for unity gain.

Simulation indicates two significant poles. The first pole, at 10MHz, is produced by the second gain stage transistor (Q11, in Fig. 3.4) and the second at 100MHz produced by the differential pair.

The poles created by the follower buffers lie near 10GHz and are therefore of no concern.

Phase lead compensation involves placing a zero at the dominant pole frequency, thus effectively eliminating it. However, a pole must also be created to achieve this. This pole can nevertheless be placed at such a high frequency that its effect on stability is negligible. A simple RC network provides the pole and zero.

It is necessary to reduce the gain of the differential pair to shift the entire magnitude response downwards. This is achieved by separating the transistor loads of the differential pair as in Fig. 3.3. The resulting compensated response is shown in Fig.3.4. The effect of the zero in restoring the phase is
4 SIMULATION

Some of the more important results of SPICE simulation are presented in Table 4.1 with those of another GaAs op-amp [1] for a comparison. However, a direct contrasting is not appropriate because of the differing design goals in the circuits. A notable general observation is the poor dc characteristics of GaAs devices compared to Si. A second important limitation of GaAs analogue devices is the increased low frequency noise - due to its higher 1/f noise corner (~1MHz). Fig. 4.1 shows the unity gain step response at 100MHz.

5 APPLICATIONS

The high speed operation of the GaAs op-amp opens up new applications in GaAs integrated circuits. It will permit the design of mixed analogue/digital systems in GaAs such as high speed signal processing and communications chips. One of the most useful new applications created by the op-amp is for Switched Capacitor Filter (SCF) circuits. Si SCFs are limited to a maximum signal frequency of around 50kHz, by the bandwidth of the Si op-amp. GaAs op-amps relax this restriction and examples of GaAs SCFs operating at 10MHz are available in the literature [7]. This opens up the Radio Frequency range to SCF applications.

6 CONCLUSION

This paper has presented a GaAs operational amplifier which improves on the performance of existing devices. It conforms to the CSIRO fabrication process design rules. Computer simulation indicates an open loop gain of 75.8dB and a unity gain bandwidth of 2.5GHz. Such an improvement is made possible by limiting the complexity of the circuit at the expense of other performance characteristics. The circuit is suitable for application in large high speed IC designs and is not intended to be used as a stand alone device.

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8 REFERENCES

Switched RC modelling Technique for GaAs Digital Circuits

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A simple switched capacitor, resistor model allows rapid yet accurate simulation of large GaAs BFL switching circuits. Such a model is developed and tested against a SPICE reference model. A benefit gained from the process of extracting the model is the insight into the exact operation of the individual gate elements.

1. INTRODUCTION

A switching circuit, such as a Buffered FET Logic (BFL) system, can be accurately simulated with a discrete SPICE element for each component but can require a large computational effort. The simulation can be simplified by assuming that each node in the circuit is affected by a simple switching action described by a current source and admittance with values dependent on the node potentials. In addition, time delays can be modelled by including appropriate capacitance elements. In a digital system, these components, at any instant, have one of only few values and so the computational effort is greatly reduced. To improve simulator convergence and speed the circuit topology can be further simplified by disallowing the use of node-to-node components.

The BFL gate is relatively complex as it includes the level shifting buffer stage required in Gallium Arsenide circuits using only depletion mode devices. The buffer stage includes a source follower and pull-down transistor and a diode level shifter. The logic stage includes a pull-up transistor and switch transistors. The development of a switch model for this gate requires the substitution of devices fulfilling a range of functions and the techniques are applicable to other logic families using fewer device functions.

2. THE SIMPLE MODEL

A switching model can be found by considering each element in a logic gate and its influence on the external nodes of the gate. An accurate and detailed SPICE simulation serves as a reference [1] and each device’s SPICE model substituted, one at a time, by a simple model based on a hypothesis of how it influences the circuit. Each effect is then investigated by adding or removing it from the simple model to confirm that it is as hypothesized. This method isolates and highlights the critical components and their effects on the circuit, giving clear insight into its operation.

The starting point for developing a simple model is a set of transistor characteristic curves (Fig. 2). These can be modelled by a set of linear functions which follow the basic parameters of the device. In the saturated mode, the drain conductance is constant and the current is proportional to the gate bias. In the linear mode, the drain conductance is higher and its modelled value is selected to adequately cover the range of operation for each device depending on its function.

2.1. Diode Chain

The simplest component in the BFL gate is the diode chain which can be described by a standard small signal model. This consists of a resistance, $R_d$, and voltage, $V_d$, connected in series with a parallel capacitance, $C_d$. The effective capacitance is made up of the parasitic component and the junction capacitance which is isolated from the diode’s external terminals by a parasitic series resistance. In order to further simplify the model, this capacitance can be represented by one in parallel with the pull-down.

Figure 1: Basic Buffered FET Logic (BFL) Gate. Logic functions are created by various combinations of single and dual gate switches.

Figure 2: Basic characteristics of FET device. A simple model is a linear approximation to the operating regions.
2.2. The Pull-Down Transistor

The pull-down transistor is generally operated in the saturated mode as a constant current source for the diode chain. An adequate model of this transistor is a parallel combination of a current source, $I_{pd}$, and a conductance, $G_{pd}$. However, when the logic gate output is low, it operates in the knee region between the saturated and linear modes. Thus the model has two states depending on the relation of drain potential to a critical knee voltage as shown in Fig. 3.

The parasitic drain resistance of the device is negligible, so the equivalent parallel capacitance is the sum of the parasitic interelectrode and the gate-drain junction capacitances.

2.3. Source-Follower Transistor

The source-follower can be modelled by a series voltage and resistance. In this case the voltage source contains both a dc component, $V_{sf}$, which includes the power supply, and a component proportional to the gate-source potential with gain, $A_{sf}$. In the saturated mode, the gain is the product of the transconductance and the drain-source resistance. In the linear mode the drain-source potential is proportional to the gate-source potential so the drain-source resistance is selected for correct proportionality rather than to follow the transistor characteristic (Fig. 4).

The drain-source parasitic capacitance is transformed to an equivalent capacitance at the buffer stage output and the gate-drain capacitance remains at the buffer stage input. The effect of the gate-source capacitance is dependent on both the input and output of the buffer stage.

2.4. The Buffer Stage

The buffer stage can be assembled to form a single switched node $V_{out}$ controlled by an input node $V_{in}$ (Fig. 5a). The equivalent output node current and conductance is given in equation 1. This may look complicated but it is simply a three region piece-wise linear function of the input and output potentials. The dc transfer characteristic displays a constant level shift with unity gain in the main region of operation. At either extreme, there is a saturation effect as either the pull-down or source follower move into the linear mode of operation as shown in Fig. 5b.

$$I_{bf} = \frac{V_{sf} + V_{d}}{R_{sf} + R_{d}} + I_{pd} - \frac{A_{sf} (R_{d} V_{sf} - V_{d} R_{sf})}{R_{sf} + R_{d}(1 + A_{sf})} + \frac{A_{sf} V_{in}}{R_{sf} + R_{d}(1 + A_{sf})} \quad (1.a)$$

$$G_{bf} = \frac{1 + A_{sf}}{R_{sf} + R_{d}(1 + A_{sf})} + G_{pd} \quad (1.b)$$

The capacitance at the output is the sum of the contributions from each device.

The capacitance at the input is dominated by the equivalent Miller effect capacitance of the source-follower gate-source junction. To model the behaviour of the buffer over an entire high-low-high cycle this capacitance must take on several values. It is also important to include the effect of the source follower’s parasitic source resistance which is significant in the linear region where the output is at a high potential and the gate-source junction is forward biased. This reduces the effective junction capacitance. When the output is lower, the parasitic resistance is not significant and the simple sum of the parasitic and junction capacitances can be used.

Referring to Figs. 5b, 5c and 5d, during the initial part of a falling transition the gain is high because the output potential lags the input and so the Miller effect capacitance is large. As the input falls a region of moderate gain is passed and so the Miller effect is also moderate. The capacitance then reduces to a low value in the region of unity gain before finally reverting to a moderate value as the gain of the buffer reduces because the Pull-down transistor saturates.

At the start of a rising edge, the effective input capacitance is moderate while the pull-down is in the linear mode and the buffer stage has less than unity gain. During most of the rising edge the input capacitance is small because the buffer has near unity gain. At the top of the rising edge the capacitance
rises as the source follower gate junction runs into forward bias condition and the gain of the buffer reduces. This region is passed momentarily and does not have a substantial influence.

Because the input capacitance value is dependent on the output potential of the gate the input is correctly affected by any output loading which slows down the circuit. The region of unity gain needs to be chosen so that the correct Miller effect capacitance is applied as the gate loading changes. Loading the gate or fast input transitions have the effect of increasing the output verses input hysteresis loop as shown in Figs. 5c and 5d. The shaded area in these diagrams shows the unity gain regions selected for correct response to gate loading.

This description of Miller effect capacitance explains why the fall delay of the gate exceeds the rise delay. That is, when the gate junction of the source follower is forward biased stored charge in the channel of the device must be removed before a falling transition can occur. This is represented by the high Miller effect capacitance at high output levels. This also suggests that the gate delay can be reduced by not letting the source follower (and the pull-down transistor) operate in the linear region.

2.5. Pull-Up Transistor

In a similar manner to the pull-down transistor, the pull-up operates in both the saturated and linear modes. The main difference in the dc model is that the entire linear region is modelled rather than just the knee region as shown in Fig. 6 (cf. Fig. 3).

2.6. The NOR Switch Transistor

The switch transistor can be modelled by a current source and a parallel conductance with a transconductance from the gate to the drain. Near the logic threshold the transistor has a relatively low transconductance. However, to properly simulate the charging characteristics of the device when the gate potential is high it is necessary to have a higher transconductance so that the correct high drain current is produced when the gate potential is suddenly raised. The model shown in Fig. 7 achieves this with a two piece description of transconductance.

A delay normally occurs before the output rises because it is slightly lowered by the falling input through gate-drain capacitance. Since a node-to-node element is being avoided in the simple model, the gate-drain capacitance can be added to the output drain-source capacitance to delay the initial rise of the output. It turns out that this capacitance is critical to correct timing and suggests that the drain node should be the subject of careful circuit layout for maximum speed.

The effective input capacitance is a complicated function of the input and output potentials. When the switch is pinched-off there is a low capacitance made up of the gate-drain and the gate-source capacitance. In this case the gate-source junction capacitance has a value similar to the gate-drain junction capacitance. When the switch is not pinched-off, the gate-source junction capacitance increases. There is also a large Miller effect capacitance which is significant during the high gain region of an output transition. This should be calculated from the gain of the switch/pull-up combination.
2.7. The NAND Switch Transistor

The NAND Switch is a dual gate FET which can be modelled as two FET’s in series. The lower FET is effectively a controlled source resistance for the upper FET which reduces its effective transconductance by a factor $K$. The drain current is the minimum that the two FET’s will each allow. This can be modelled by a single gate FET controlled by the minimum of the upper gate potential and the lower gate potential scaled relative to the pinch-off potential, $V_{po}$,

$$V_{gs} = \min(V_{gs_{upper}}, KV_{gs_{lower}} + (1-K)V_{po})$$

Each gate’s input capacitance is the same as for the single gate model except that the Miller component is not present at the lower gate. In addition, when the lower gate causes an output transition, it must also charge the upper gate junction. This loading is equivalent to an extra capacitance added to the logic stage output capacitance during the rapidly rising or falling part of a transition. This clearly identifies the reason why the lower gate is a slower input to an AND gate.

3. A TYPICAL APPLICATION

The process of constructing a stick model for the gate has been automated. The reference SPICE model is used to probe each device in its actual operating environment. A SPICE version 3 program automatically analyses the circuit and produces raw data which is then ported to a formatting routine to produce the simple model. For the purposes of testing, the simple model is built up using SPICE circuit elements and switches. The formatting routine can produce C code for use with the simulation Jig [2] or similar logic simulator.

The performance of the simple model is demonstrated by the ring oscillator, cyclic counter circuit shown in Fig. 8. Critical timing is demonstrated by the ring oscillator and all combinations of input transitions by the AND/OR gates used in the latches. The simple model is in excellent agreement with the SPICE reference model and is able to reproduce the minor ringing after the transitions.

4. CONCLUSION

A switching circuit, such as a GaAs BFL gate, can be accurately simulated by assuming that each node in the circuit is affected by a simple switching action described by a current source and admittance with values dependent on a control node.

The main purpose for creating the simple switched model is to give the designer a means for rapidly simulating large complex circuits. However, a significant benefit gained from the process of extracting the model is the insight into the exact operation of the individual gate elements. For example, the speed reductions due to the saturation of the buffer stage and the speed variation between AND inputs are identified and explained. With this information it is possible to design and improve the circuit and its topology so that maximum speed is achieved.

5. ACKNOWLEDGEMENT

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6. REFERENCES

AUTOMATIC DESIGN OF GaAs DIGITAL CIRCUITS AND DEVICES
FROM PROCESS AND MATERIAL PARAMETERS TO LAYOUT

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ABSTRACT
Sydney University Electrical Engineering and CSIRO Division of Radiophysics have collaborated over the past three years to develop digital circuits by design tools needed to design digital circuits for MBE processes geared to low noise microwave and millimetre wave applications. The design approach commences with input of the fundamental process parameters and design rules. From these, SPICE models suitable for use in the design of both linear and digital circuits are automatically generated. These, in turn, are used to automatically design and layout basic logic gates. Simplified models of the gates are extracted for use with a mixed-mode simulator. This entire task from designer entry of parameters, through generation of accurate and simplified models, to layout, can be completed in less than 90 minutes. This paper gives an overview of the design process, describes each of the key problems that had to be addressed in its automation, and shows results of a fabricated circuit.

INTRODUCTION
The major part of the start-up effort in designing GaAs digital integrated circuits for a new technology is in the creation of re-useable resources including model and layout libraries of devices, logic gates and common standard cells. Even relatively minor technology changes may necessitate alteration or complete re-creation of these resources. During our development of digital circuits, the continuing evolution of the fabrication process has dictated a resource development approach that readily accommodated change. The design system described here is our tool for automatically creating circuit design resources.

DESIGN TOOLS AND STANDARD LIBRARIES
Fundamental to the digital circuit design process is the set of CAD tools used to assemble and simulate circuits. Simulation tools use appropriate device and circuit models, and layout tools use fabrication design rules. Small custom cells and circuits are designed using discrete device models with the aid of an accurate physical level circuit simulator. Larger circuits require a system level simulator using simplified models.

The CAD tools draw on a library containing appropriate models for simulating a circuit and a set of subcells for laying out the chip mask. The library includes a standard set of logic functions with a range of power and speed characteristics. Each library element is represented in three forms: a physical simulator model based on discrete devices, a system model for rapid large-circuit simulation, and a mask layout description. Also required is a set of discrete device models for the design of custom elements and for use with the library physical models.

The basic tools used in our system are:

- **SPICE**. The SPICE [1] circuit simulator uses device or physical level modeling. Library cell models and a set of device models including parasitic elements are used for designing custom circuits and for the development of system level models.

- **Simulation JIG**. The Simulation JIG [2] is a mixed-mode (analogue/gate/behavioural) simulator. It uses simple models that represent the active circuit elements between an input node and an output node by a current source, a conductance, a capacitance at the output node and a capacitance at the input node. These components have values which are simple piecewise linear functions of potentials at the output and input nodes. This provides a rapid system-level simulation and uses the simple system-level models for each basic gate element in the cell library.

- **Magic**. The mask layout tool, Magic [3], includes design rule checking and circuit extraction functions. It can be used to layout custom circuits (including library cells) and assemble subcells from the circuit library. The design rules for the fabrication process are used by the checking and extraction routines.

DESIGN APPROACH
The design system follows a logical design flow from fundamental parameters through to an automatic design of logic gates. Design commences with the input of fundamental material and process parameters, and design rules. This starting point gives flexibility for adapting to a fundamental change of technology and provides a means to consider the affect of process variations on the final circuit elements. Sensible default parameters are available at all stages so that the designer may take up the design sequence at any stage. Moreover, derived (calculated) values may be over-ridden by those obtained from measurement. If the process is known, the appropriate parameters can be entered and device models will be generated. If measured device parameters are available, the process parameters can be by-passed and the design sequence can start with entry of the device descriptions.

Implementation of the design system required the development of the rules and procedures for creating device descriptions...
and circuit elements from fundamental parameters. Hence, the parameters which define the fabrication process had to be identified. Also, it was necessary to supplement the design tools noted above with specific models and routines for handling the new devices and GaAs technology.

**Process Dependent Parameters**

Starting with the fabrication process parameters provides three advantages. Firstly, because the design sequence is automated, a change in the fabrication process can be painlessly reapplied to update an entire circuit library. Secondly, the design sequence starts at a fundamental level so it can be quickly adapted to a fundamental change such as a change of material, from GaAs to InP for example, or moving from a MESFET to a HEMT technology. Thirdly, the design system becomes a valuable tool for determining the effect of process variations on the final circuit elements.

The fundamental parameters listed in Table I can be divided into three categories: material dependent, process dependent and design dependent.

**Material Parameters.** The crystal and electron transport properties of the material, be it silicon or a III-V compound are required to determine the electrical behaviour of the devices manufactured with it. These properties are not affected by subsequent fabrication steps. However, they are affected by design parameters such as the choice of nominal doping level, so the design system must be able to predict these influences.

**Process Parameters.** Process changes affect the quality of Schottky junctions and ohmic contacts. The Schottky metal chosen is significant and its properties are required to predict Schottky barrier heights and ideality. Alloyed ohmic connections vary with the contact geometry so several parameters measured from process samples are required to predict contact resistance [4]. Also, the minimum electrode spacing is restricted by the alignment and lithography tolerances. These parameters are dictated by the capabilities of the fabrication process and they are independent of the type of device constructed with the process. Mask layout design rules are also dictated by the process.

**Design Parameters.** Devices used for a particular circuit can be tailored to the application by setting the design parameters. MESFET pinch-off potential, for example, is adjusted by setting the channel depth. Parasitic resistances and capacitances are affected by the device geometries and trade-offs with power and circuit density go with the selection of these parameters.

**SPICE Models**

The devices available are the Schottky barrier diode, MESFET, HEMT and various passive components. While the existing diode and passive component SPICE models are adequate, the FET models require enhancement for application to GaAs FET’s. In the current version of SPICE, the JFET and MESFET models were modified to obtain accurate predictions for MESFET’s and HEMT’s [5-6]. Second-order effects and careful matching of the small signal models have produced reliable models that can be used as a substitute for a fabrication test run. The need for detailed modeling was critical because it was necessary to predict circuit behaviour using processes which had not yet been fully developed.

**Gate Design Procedure**

To automate the basic gate design procedure, a design sequence was developed which considers designer specified power/speed trade-offs and constraints on specification of power supplies, logic swings and circuit size. The sequence produces a parameterised topological description of a family of logic gates which can be passed to a parsing routine to create gate library subcircuits. These, in turn, are used in combination with designer trade-off goals to automatically design and layout each gate in the library. The SPICE models are reliably used as the basis for extracting device parameters used in the design sequence. An automatic SPICE-based procedure also uses the SPICE device models and gate subcircuit descriptions to derive a set of simple models for the Simulation JIG [7].

**DESIGN SYSTEM IMPLEMENTATION**

The design system is the bridge between the fabrication process and the set of model descriptions, standard circuit elements and layout cell. The core of the system is a PC-based front-end software package, GaAsSPICE, which maintains a database and provides an interface for designer interaction. Additional packages produce the Simulation Jig models and mask subcells (See Fig. 1).
GaAsSPICE

GaAsSPICE has a highly modular structure in which a main engine invokes separate script files and calculation routines as needed. This flexible arrangement isolates independent design activities and facilitates rapid change of the design steps. For example, changes in circuit topology or subcircuit requirements are made simply by updating the appropriate script file. New simulators are accommodated by changing the parsing script to produce models in an appropriate format.

The fundamental process parameters are entered in three stages: the first for material properties, the second for process parameters (which are constant for a given process), and the third for design parameters.

From these are automatically generated accurate SPICE analogue device model descriptions suitable for use in the design of both linear and digital circuits. The user can enter the device characteristics or allow GaAsSPICE to calculate them from the fundamental parameters. Specifically, the diode and MESFET model parameters are listed with an option to over-ride each.

The device descriptions are used as an input to an automatic gate design system. At present this produces and stores in the database those parameters which give the ratio of device sizes within a BFL gate. The design parameters can be adjusted in order to obtain the desired circuit performance.

The final step creates the SPICE 'include' files of gate libraries and model cards for various process settings and, additionally, produces a set of parameters which can be used by further processing routines to generate the JIG system level models and layout cells.

Calculating. GaAsSPICE performs a triple set of calculations to give models for a nominal condition, a high temperature extreme and a low temperature extreme. The designer can over-ride the nominal result and extreme cases are automatically calculated as a deviation from this result. The extreme case models are calculated from the set of extremes of parameter values specified in Table II.

Gate Design. An interactive gate design routine is used to produce a reference logic gate. The extreme of logic levels expected with process and environment variation are graphically given so that the user can check that the design parameters result in an effective circuit over all process and environment tolerances (See Fig. 2).

The design procedure uses simple piecewise approximations to the devices to iteratively design an optimum circuit based on dc logic levels and noise margins. The circuit is also optimised for maximum speed based on the user nominated fanout.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Low Model</th>
<th>High Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>Temperature</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>r_h</td>
<td>Ohmic Sheet Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>r_c</td>
<td>Ohmic Contact Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>a</td>
<td>MESFET channel depth</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>N_d</td>
<td>Nominal doping Level</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>d_s</td>
<td>Diode electrode spacing</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>d_g</td>
<td>MESFET electrode spacing:</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

Table II: Assignment of Parameter Extremes

RC Models

A system-level model is produced with the aid of a script program that drives SPICE and interprets its output. This uses a basic gate circuit to characterise each active component in the circuit. The transconductance and resistance of each device is approximated over its actual operating range and the device is substituted by a simple current source and conductance. The substituted devices in a basic gate are then assembled and simplified into a single current source and conductance for the gate. A parsing script is used to produce a listing of the simple models in an appropriate form for the Simulation JIG.

Mask Layout

An automatic layout package uses the basic gate description produced by GaAsSPICE to create CIF subcells for each circuit in the model library. The cells follow a standard layout and the relative size of each component is adjusted as required. These subcells can be assembled with Magic and a set of process design rules is used for layout checking and circuit extraction.
The entire task from designer entry of parameters, through generation of accurate and simplified models, to layout, can be completed in less than 90 minutes. The inverter circuit shown in Fig. 3 was designed with GaAsSPICE using the parameters for a MBE mesa process developed at the CSIRO Division of Radio-physics [8]. The circuit models for the nominal and two extremes were used to simulate the responses shown in Figs. 4 & 5. A typical CIF layout is shown in Fig.3. The inverter was fabricated and the measured results are shown.

**CONCLUSION**

The design system presented here is a bridge between the fabrication process and a set of model descriptions, standard circuit elements and layout cells. It can be quickly adapted to a fundamental change in technology and therefore is a valuable what if? tool for determining the merits of a process modification. The designer may take up the design sequence at any stage and may freely over-ride internally calculated parameters. User specified power/speed trade-offs and design constraints are used to automatically design and layout basic logic gates. SPICE models suitable for use in the design of both linear and digital circuits are generated and simplified models of the gates are extracted for use with the JIG mixed-mode simulator.

The design sequence is automated and can be easily repeated under the control of the PC-based front-end software package, GaAsSPICE. The modular structure of this package facilitates rapid change of the design steps. Thus, it will be a useful aid in the rapid application of new technologies.

**REFERENCES**


An Improved FET Model for Computer Simulators

ANTHONY E. PARKER and DAVID J. SKELLENN

Abstract—An alternative simple description of FET drain current provides the flexibility of an extra parameter which can be chosen to approximate the Shockley expression or general power law. An empirical polynomial expression which uses only integer powers is used to provide computational efficiency. The new expression gives the designer a more accurate FET model which is consistent for both large- and small-signal simulations.

The JFET and level 1 MOSFET dc models in SPICE [1] use a simple square-law relation which often does not precisely fit real device transfer characteristics. The predicted small-signal behavior is valid only in regions where the square-law matches measured large-signal behavior. Designers using SPICE often have to make adjustments to circuit bias points or device parameters to reconcile any differences. Better results can be achieved with general power law relations [2] or the Shockley equation [3], but these are not desirable in software simulators because they are computationally intensive expressions. Thus there is a need for an expression which is computationally simple and yet provides an accurate fit to measured data.

Here we describe an improved simple description of FET drain current which provides the flexibility of an extra parameter that can be chosen to approximate the Shockley expression. This parameter is easily fitted to measured data in the same way as the exponent in Richer and Middlebrook’s general power law relation [2]. The new expression gives the designer a more accurate FET model which is consistent for both large- and small-signal simulations.

Recall that the basic FET has between source and drain electrodes a doped semiconductor channel which is controlled by depleting the channel region under a gate electrode with a gate-source bias, Vgs. The device operates in three modes. In the linear mode, the drain-source voltage, Vds, is proportional to the gate-source voltage, Vgs. As Vgs increases, the device enters the saturated mode where the current ceases to rise, because at the drain end, the channel is completely depleted, or pinched-off. The third mode is a cutoff mode where no current flows because the channel is completely depleted.

As used in the Shichmann-Hodges model [4], Shockley’s expression is generally accepted as the standard description of FET

\[ I_d = \beta (V_{gs} - V_{th})^2 / (3d^2 - s^2) \]

where \( s = \sqrt{(V_{gs} - V_{th}) / (V_{gs} - V_{ds})} \) and \( d = \sqrt{(V_{gs} - V_{th}) / (V_{gs} - V_{ds})} \) are the extents of channel depletion at the source and drain ends, respectively, \( V_{th} \) (volts) is the gate-source potential required to deplete the whole channel of carriers, and \( V_{th} \) is the gate junction built-in potential (volts). The use of a half-power-law for the terms s and d is derived by assuming uniform doping profile in the channel.

An alternate model is the general power law of order n. The drain current in the saturated mode is empirically derived, and is justified by its flexibility and good fit to real devices [2]:

\[ I_d = \beta (V_{gs} - V_{th})^n . \]

The exponent term gives the degree of freedom required to fit the model to nonuniform doping profile. Like the Shockley relation, this requires a nonintegral power function which renders it unattractive for software circuit simulators.

The simple three-mode model used in SPICE is based on a square-law function of gate bias which can be derived by assuming the electric field is constant along the channel [5]:

\[
\begin{align*}
\text{cutoff mode, } & V_{gs} \geq V_p , \\
I_d &= 0 \\
\text{linear mode, } & V_p < V_{gs} < V_{ds} , \\
I_d &= \beta (1 + \lambda V_{ds}) V_{ds} \left\{ 2(V_{gs} - V_{th}) - V_{ds} \right\} \\
\text{saturated mode, } & V_{ds} < V_p < V_p + V_{ds} , \\
I_d &= \beta (1 + \lambda V_{ds}) (V_{ds} - V_{th})^2
\end{align*}
\]

where \( \lambda = (A - V_p^{-2}) \) is a transconductance parameter and \( \lambda V_p^{-1} \) is a channel-length modulation parameter. This expression is computationally efficient but does not provide as good an agreement, with real devices as a general power law or the Shockley expression.

Our alternative model is derived from the Shockley expression by applying a third-order Taylor expansion to the radicals, \( d^2 \) and \( s^2 \) (in (1). Like terms are collected and their coefficients replaced by constants A and B. The result is a simple extension to the SPICE relation:

\[
\begin{align*}
\text{cutoff mode, } & I_d = 0 \\
\text{linear mode, } & I_d = \beta (1 + \lambda V_{ds}) V_{ds} \left\{ B (2V_p - V_{gs}) + A \left[ V_{ds}^2 + 3V_p (V_{gs} - V_{th}) \right] \right\} \\
\text{saturated mode, } & I_d = \beta (1 + \lambda V_{ds}) V_{ds} \left\{ B + A V_p \right\}
\end{align*}
\]

where \( V_p = V_{ds} - V_{th}, A = (1 - B) / (V_{gs} - V_{th}) \), and \( 0 \leq B \leq 1.2 \) is a fitting parameter. The range of B is restricted to eliminate regions of alternate transconductance.

A convenient degree of freedom is provided by the term, B, which can be considered as the “doping profile parameter” because it allows deviation from Shockley’s uniform doping assump-
Fig. 1. The similarity of the new model to a general power law, solid lines, is shown for \( n = 3 \) (●); \( n = 2.4 \) (×); and \( n = 1.8 \) (○). In all cases, \( \phi_o = 0.7 \) V, although the sensitivity to this parameter is very low.

Fig. 2. The new model is a much better fit to experimental data (×), than the square-law SPICE model. The FET's shown in Figs. 3 and 4, follow power laws with exponents, \( n = 2.34 \) and \( 2.39 \) and pinch-off potentials, \( V_{to} = -1.89 \) and \( -0.98 \) V, respectively.

Fig. 3. The experimental data (×), is shown for a GaAs FET with gate length 100 \( \mu \)m and width, 200 \( \mu \)m. The new model (4) is shown by solid lines with parameters \( \beta = 330 \mu A \cdot V^{-2} \), \( V_{to} = -1.89 \) V, \( \beta = 6.6, \lambda = 13 \) mV\(^{-1}\), and \( \phi_o = 0.7 \) V. This provides a better fit than the square-law SPICE model, (○○○○), with parameters \( \beta = 299 \mu A \cdot V^{-2}, V_{to} = -1.89 \) V, and \( \lambda = 13 \) mV\(^{-1}\).
tion. When \( B \) is set to 1, the original SPICE square law is exactly implemented and when \( B \) is set to 0.60, the model is a very close approximation to the Shockley expression. Typical values of \( B \) range from 0.3 to 0.4 for a doping profile with an extended tail, through 0.6 for a uniform profile, to 0.9-1.1 for a negative gradient profile.

The essential features of a FET model are present in the new expression. The model is a well-behaved differentiable function and crosses the device's operating mode boundaries smoothly. The drain conductance at saturation and the transconductance at pinch-off are zero as expected. Also, the small-signal transconductance, \( g_m \), and zero bias drain-source conductance, \( G_{ds,0} \), are equal so the model still obeys the known result that the transconductance at zero-gate voltage is equal to the total channel conductance in the absence of the gate structure" [4]:

\[
g_m = G_{ds,0} = \beta V_C \left\{ 2B + 3AV' \right\}.
\]  

(5)

In fact, the new expression for saturated drain current, (4c), very closely follows a general power law relation of order \( n = \frac{3-B}{B} \). This can be demonstrated with a property of a general power law expression that Richer and Middlebrook [2] used and supported with measured data. That is, the ratio of the saturated drain current and transconductance is a linear function of gate bias:

\[
\frac{I_{DS}}{g_m} = \frac{\beta V_C^2 [B + AV']}{\beta V_C [2B + 3AV']} = \frac{1}{3-B} (V_{GS} - V_{TH}).
\]  

(6)

As shown in Fig. 1 the approximation (6) is very close. Thus the validity of the new model is substantiated by its resemblance to the already justified general power law. The advantage of the new expression is that it does not use a computationally intensive radical function.

When applying the new model to measured data, the necessary parameters can be easily determined once the effects of drain and source parasitic resistances are removed. The pinch-off voltage and doping profile parameters can be graphically determined from a plot of the ratio of drain current to transconductance [2]. The channel-length modulation parameter can be determined from the saturated mode drain-source conductance and the transconductance parameter chosen for best fit.

Application of both the SPICE square-law model and the new model to measured data is shown in Figs. 3 and 4. A silicon FET type NF510 and a Gallium Arsenide (GaAs) Schottky barrier FET (MESFET) of planar construction with gate dimensions 100 \( \mu \text{m} \) long by 200 \( \mu \text{m} \) wide were used. The ratio of saturated drain current and transconductance of these device is shown in Fig. 2 and from this, the doping profile and pinch-off parameters were determined. Note that the departure of the ratio from the straight line near pinch-off is due to drain leakage current.

It can be seen that applying the new model gives an excellent fit to the experimental data. The square-law model is not as good but still provides a reasonable large-signal model. Of more significance is the inability of the square law to properly relate the small-signal transconductance to drain current as shown in Fig. 2. To use the square-law model, it is necessary before performing a simulation to select the pinch-off potential and transconductance parameters to suit the purpose of the simulation. A best fit to the large-signal behavior can correctly predict the operating point but not necessarily the small-signal gain at that point. Before performing a small-signal analysis the model parameters must be adjusted or the bias point moved to a region with correct small-signal gain.

The advantage of the new model over the square-law model is that it can more accurately fit the large-signal behavior of a device, and therefore, consistently predict small-signal behavior over an extended operating range. It can correctly relate the small-signal transconductance to drain current and so eliminate the need for inconvenient juggling between large- and small-signal model parameters.

In summary, an improved JFET model suitable for computer simulators has been presented. It uses a simple polynomial extension of the existing SPICE model which allows a very good fit to the standard Shockley expression and also features the flexibility of a general power-law without using a computationally intensive radical function. There is an extra degree of freedom in the form of the "doping profile parameter" which allows the model to correctly relate small- and large-signal behavior.

REFERENCES


9.3 GaAsSPICE Manual

The *GaAsSPICE* program is a major design tool for the development of a GaAs digital logic cell library. The manual reproduced here is the same as used by members of the GaAs Integrated Circuit Project Team as a reference for applying the simulation tools and preparing library cells for circuit layouts.
GaAs SPICE

Computer Spreadsheet Program
for extracting GaAs Schottky Diode and MESFET model parameters
and designing Buffered FET Logic Gates
with SPICE

Version 2.0

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May 1989

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Gallium Arsenide Digital Integrated Circuits Project
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GaAsSPICE

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Introduction

The GaAsSPICE spreadsheet program is designed to aid in the selection of parameters for GaAs integrated circuit simulations with the popular SPICE program. It consists of a set of worksheets which process basic crystal and electrical properties of Gallium Arsenide integrated circuits. The aim is to use these properties to estimate the basic SPICE parameters for the MESFET and Diode models and the Sydney University modified JFET model added to SPICE version 3b1. GaAsSPICE produces text files which can be included in the circuit description deck.

GaAsSPICE also includes a digital gate library and design facility. It will automatically design a logic gate using the device descriptions that it determines. Then gate libraries can be compiled into text files suitable for inclusion into a simulation.

This manual serves as a guide to using GaAsSPICE and provides information for understanding the detail of its operation. The first section describes the format of the various parts of the spreadsheet as presented to the user and the data that must be entered. In the second section, a detail listing of formulas with references is given. This section can be consulted if more detail about user entered parameters is required. It is recommended that the reader obtain a SPICE manual to assist in following the use and purpose of the parameters returned by GaAsSPICE.

Features

- GaAsSPICE requests a set of process dependent parameters to use as the basis for predicting device properties.
- Measured parameters may be entered at any stage in GaAsSPICE’s calculation.
- Model cards for both the MESFET and the Schottky diode are provided.
- Specification of temperature for temperature analysis. This is necessary because SPICE 3b1 does not perform temperature analysis.
- Plotting routines for optimising diode and MESFET parameters are provided.
- Separate worksheets for designing Buffered FET Logic gates are included.
- Generates gate libraries for inclusion in SPICE simulations.
Installation

The GaAsSPICE distribution comes on one 3.5" floppy disk containing the GaAsSPICE startup file and the GaAsSPICE folder which contains the working files and the GaAsSPICE Engine. A demonstration version of the Microsoft Excel spreadsheet program is also included. This will allow GaAsSPICE to run but will not allow any writing or saving to disk.

To install the system on a hard disk, copy the GaAsSPICE folder to some convenient directory (e.g. the System Folder) and the GaAsSPICE startup file to any working directory where the output files from GaAsSPICE should appear. There can be any number of GaAsSPICE startup files distributed in the directory hierarchy.

To run GaAsSPICE open the GaAsSPICE startup file and the program will automatically begin execution. If the GaAsSPICE folder cannot be found, the user will be given the opportunity to look for it and its location will be remembered by that copy of the startup file. The welcome dialogue should appear.

When starting GaAsSPICE, the user is presented with the option either to use the default data or to open a previously saved data file. If there is no previously saved data, select the default data option. If the 'Open Data' option is used and then cancelled, default data will be used. When a selection is made the main menu is presented.
Operation Guide

General Techniques

*GaAsSPICE* presents a sequence of ‘Dialogue boxes’ that prompts the user for information. Each box has a *help* button which will give a short description of the functions available in that box.

In all cases where *GaAsSPICE* calculates a parameter, there is an option for entering another quantity so that the calculation is overridden. In the dialogue boxes, calculated quantities have a square ‘Check Box’ associated with them. When the ‘Check box’ is blank, the calculated quantity will be shown and the user will be able to edit the value. However, the edited, or entered, value will be ignored unless the ‘Check Box’ is marked with a cross. If the user changes the quantities and wants *GaAsSPICE* to recalculate, the ‘Dialogue Box’ should be closed and reopened from the main menu.

If the ‘Dialogue Box’ is closed by using the *OK* button, the entered results, with marked ‘Check Boxes,’ will be used for the recalculation. If the *Cancel* button is used, the original state of the ‘Check Boxes’ will be used.

*GaAsSPICE* performs its calculation in triplicate: to give results for a nominal condition, a high temperature extreme and a low temperature extreme. The user can only override the nominal result. The extreme cases are calculated as deviation from the nominal result using the trend predicted by the GaAsSPICE internal formulae.
GaAsSPICE main menu

The main menu options are organised in order so that the user can work down the list, starting with entry of basic data and finishing with creating complete SPICE library files. As usual, there is a help button.

The functions available are

Set Crystal Properties - This is rarely used but allows the user to set fundamental physical constants such as relative permittivity.

Set Process Parameters - Set parameters which are constant for a given process (e.g. contact resistance).

Set Design Parameters - Set parameters, such as pinch-off potential, which are determined by design.

Diode Model - Check the SPICE diode model Parameters.

MESFET Model - Check the MESFET model Parameters.

Design BFL Gate - Design a Buffered FET Logic gate library.

Create SPICE Deck - Create the SPICE 'include' files with model cards for various process settings.

Save Parameters - Save or Load all parameters to files.

The remainder of this operation guide will describe each main menu item and the use of the 'Dialogue Box' presented by each. More information on how to choose and interpret the quantities and data is given. Detail description of GaAsSPICE calculations and references for finding data appear in later sections.

Set Crystal Properties

Fundamental GaAs Crystal Properties, relative permittivity, density of Conduction Band States, effective electron mass and the electron velocity description parameters are entered here. These quantities are usually independent of the fabrication process and normally should not need altering.

The first three constants can be determined from published data. Several references quote 13.1 as the relative permittivity of GaAs [Nuzillat et al. 1982, Wada and Frey 1979, Sze 1985]. Some debate seems to exist in earlier references which quote between 12.1 and 13. The relative mass of an electron in the lower
conduction band valley is 0.068 [Sze 1985]. The Conduction Band State density is automatically adjusted for temperature, so the value entered here should be for 300°K. This is quoted between $4.7 \times 10^{17}$ and $5 \times 10^{17}$ per cm$^3$ at 300 K [Nuzillat et al. 1982, Sze 1985].

The electron velocity parameters are calculated by \textit{GaAsSPICE}. The low field mobility is based on a good fit to experimental data and is valid for doping concentrations between $10^{15}$ and $10^{19}$ cm$^{-3}$. Inverse temperature dependence is also included. The saturated electron velocity is calculated as a function of the low field mobility. Then the field strength for maximum velocity is calculated using both the saturated velocity and low field mobility. Finally, the maximum electron velocity is calculated from all three parameters.

The low field electron mobility and the other velocity parameters are calculated in triplicate for determining the nominal and extreme cases of temperature and doping level. The quantities shown are at the nominal temperature and doping as set in the Main Menu \textit{Design Parameters} option. The calculated quantities can be overridden by using the check boxes and entering the desired value for nominal doping and temperature state.

\section*{Set Process Parameters}

The process parameters are particular characteristics of the fabrication process that are not normally varied by design. Instead, the manufacturer constantly strives for the best results. These parameters should not need altering unless a change occurs in the fabrication process.

\textit{GaAsSPICE} can be forced to use a given Schottky Barrier Height (i.e. diode junction built-in potential) which would probably be determined by measurement of a fabrication sample. Alternatively, it can be calculated from the metal ‘work function’ and parameters for modelling the effect of GaAs Surface States at the junction [Sze 1985]. In either case the Barrier is automatically adjusted for temperature and doping in the triplicate calculation so the values entered here should be at nominal temperature and doping level.

The relative mass of electrons in the metal is required for calculation of the diode junction ideality factor.

The GaAs breakdown field affects the breakdown potential of the diode model. Tunnelling breakdown through Schottky junctions occurs at the breakdown field 200 kV/cm [Sze 1985].
Wiring connections are made by creating an alloy in the GaAs epi-layer under a metal contact. The resistance of the connection consists of a contact resistance between the metal and the alloy, the sheet resistance of the alloy under the contact and the sheet resistance of the epi-layer between the connection and the active part of the device [Marlow and Das, 1982]. The correct specification of these parameters is necessary for the calculation of parasitic resistances as a function of contact dimension. The variations specified in this 'Dialogue Box' are used in the Triplicate calculation.

**Set Design Parameters**

The design selected parameters are those which can be adjusted to suit the circuit requirements. The desired operating temperature range is also specified.

The nominal and extreme operating temperatures are used in the triplicate calculation. Note that most of the other parameters entered into the program are at the nominal temperature set here (not 300°K).

The Pinch-off potential has a process variation from device to device. This and the nominal doping level variance are also used for finding extreme cases in the triplicate calculation.

The device dimensions are usually determined by lithography and layout considerations. In GaAsSPICE the user specified pinch-off voltage is used to calculate the channel depth. The length and spacing of the device electrodes are entered by the user. These are nominally constant for the entire circuit (the device widths will be varied). The alignment error is used in the triplicate calculation to determine the extreme variation of electrode spacing. Note that ohmic lengths much shorter than the effective contact ‘transfer length’ (Lt) will have very high resistance.
**Diode Model**

*GaAsSPICE* gives the basic SPICE diode model parameters along with an estimate of their extreme values due to the process variations entered in the previous Main Menu options. These extremes are the result of the triplicate calculation that *GaAsSPICE* performs. Note that all the values are for a 1 µm wide device.

The SPICE parameters are used for the SPICE diode model card and more information on their use can be found in the SPICE manual. The parasitic capacitance is a lumped element representing the external capacitance between the diode electrodes. This should be placed in parallel with the diode in the final circuit description.

The plot button allows the user to generate a curve trace style plot for comparison with measured data. Select this option and the plot will appear with decade steps as indicated on the plot. The user can specify a device width and request a replot and also print the plot if required.

**MESFET Model**

The basic SPICE MESFET model parameters are listed along with an estimate of their extreme values due to the process limits entered in the other main menu options. Two types of models are supported and selected with the *Use JFET – Use Statz* button. When the JFET model is active, the parameters for the Sydney University Unified MESFET/JFET model are given. Otherwise the standard SPICE version 3 MESFET model (originally proposed by Statz *et al.*) is used. The model selected here will be used in the compilation of model cards in the Main Menu *Create SPICE Deck* option.
The parasitic capacitances are lumped elements representing the external capacitance between the MESFET electrodes. These should be placed externally to the device in the circuit description.

The plot button allows the user to generate a curve trace style plot for comparison with measured data. Select this option and the plot will appear with $V_{gs}$ steps as indicated on the plot.

Design BFL Gate

There are two steps to the design of the Buffered FET Logic gate element. Firstly, a simply model of the MESFET devices is defined along with the extreme variation due to process and operation conditions. Secondly, the design is produced and its performance displayed.

Device Description

The diode characteristics are determined from the diode mode parameters in the Main Menu Diode Model option. It is important that the diode model be correctly set in the Diode Model option before proceeding with the gate design.

The MESFET Device Description is entered in terms of a simple stick model fitted to the characteristic curves. The values are defined in the diagram on the next page. GaAsSPICE attempts to approximate these quantities from the MESFET model parameters calculated in the Main Menu MESFET Model option. If the user wishes to enter other values from measured devices, the Use Entered Values ‘Check Box’ should be marked.
Three values defining the resolution of size, the resolution of supply voltage and the variation in supply voltage must also be entered by the user. The transistor widths are rounded to the nearest size resolution which is likely to be limited by the mask layout tools. The nominal power supply values are rounded to the nearest voltage resolution. The user can check operation over a range of power supply variation in the triplicate calculation by entering a value for the supply variation.

When this ‘Dialogue Box’ is set correctly, select the Design Gate option and wait a few moments for an iterative calculation to finish.

Gate Design

The Gate Design Display should appear after selecting the Design Gate option. The user should adjust the width of the Pull-up transistor, the logic Swing and the nominal operating fan-out of the gate. The design is based on these three quantities.

Fan out is specified as the number of inverter loads.

Selecting the Re-Calc option will update the display which will give all the device widths and the extremes of logic levels. The logic levels can be easily checked for
extreme cases. For example, if the maximum logic threshold is greater than the minimum logic high, there will be a possibility that the logic will fail between gates with these extremes. This situation can usually be rectified by choosing a larger logic swing. It may be the case that the pinch-off potential of the devices being used limits the ability to meet a logic swing requirement.

Any of the widths and power supplies can be forced to a particular value by editing the value and marking its ‘Check Box’. This allows the user to try different designs and gain experience in the circuit behaviour.

**Create SPICE Deck**

The basic MESFET and Diode models with parasitic capacitances are formatted into SPICE include files. The models are for 1µm devices and the AREA FACTOR can be used to scale them when they are used in the SPICE circuit. In addition, a set of basic transistor elements and a logic gate library can be created as determined in the Design BFL Gate main menu option.

The user is required to select which files are required and to give a name to each file. These files will be created and will appear in the same directory as the GaAsSPICE startup file.

**Save or load Parameters**

GaAsSPICE allows the user to save the state of the spreadsheet to a file which can later be loaded back. Use the Main Menu Save option to create a data file. The user will be prompted to give a name which will be written in the file along with the date and then to give a name for the file. Also, when the user quits GaAsSPICE, the program will automatically ask if the data should be saved.

To load the data file use the Load Data option in the welcome dialogue when starting GaAsSPICE or use the Main Menu Load option at any time. Be careful that the existing state of GaAsSPICE is saved if required later before overwriting it with the Load option.
## GaAsSPICE Calculations

### Symbols and default values

<table>
<thead>
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<th>Symbol</th>
<th>Default</th>
<th>Units</th>
<th>Description</th>
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</thead>
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<tr>
<td>( a )</td>
<td>( \pm )</td>
<td>( V^{-1} )</td>
<td>MESFET Model Saturation Parm. - ALPHA</td>
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<td>( \pm )</td>
<td>( \text{Å} )</td>
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<td>MESFET Doping Tail Extending Parameter</td>
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<td>( \text{F}/\mu \text{m} )</td>
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<td>Relative Electron Mass GaAs</td>
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<td>Relative Electron Mass in Schottky Metal</td>
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<td>( \text{cm}^{-3} )</td>
<td>Density of Conduction States</td>
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<tr>
<td>( N_d )</td>
<td>( 2 \times 10^{17} )</td>
<td>( \text{cm}^{-3} )</td>
<td>Nominal Doping Level</td>
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<tr>
<td>( v_{e/m} )</td>
<td>( - )</td>
<td>( \text{cm/s} )</td>
<td>Maximum Electron Velocity</td>
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<tr>
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<td>( - )</td>
<td>( \text{cm/s} )</td>
<td>Saturated Electron Velocity</td>
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<tr>
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<td>( 1.602 \times 10^{-19} )</td>
<td>( \text{C} )</td>
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<td>( \Omega \mu \text{m}^{-2} )</td>
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<tr>
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<td>( \Omega/\text{sq} )</td>
<td>Epi-layer Sheet Resistance</td>
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<td>( T )</td>
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<td>( V_{to} )</td>
<td>2</td>
<td>( V )</td>
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<td>( \xi )</td>
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<td>( - )</td>
<td>MESFET Model Saturation Parameter - XI</td>
</tr>
</tbody>
</table>

\( \pm \) Denotes quantities calculated by GaAsSPICE
Introduction

In this section, a short description of each GaAsSPICE quantity is given along with the default value, a mathematical symbol and a reference. Where applicable, the formula used for calculated quantities is cited and referenced.

The Triplicate Calculation

GaAsSPICE performs its calculation in triplicate: to give results for a nominal condition, a high temperature extreme and a low temperature extreme. The user can only override the nominal result. The extreme cases are calculated as deviation from the nominal result, whether it is calculated or entered by the user. If the user enters a value, GaAsSPICE assumes the same dependency on process variations as its calculated value. For example, the variation with temperature of an entered value for the density of conduction states follows a 3/2 power law based on the entered value at the nominal temperature.

Throughout its calculation, GaAsSPICE keeps three sets of results. Entered values are assigned to each extreme as shown in the following table.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Low Extreme</th>
<th>High Extreme</th>
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</thead>
<tbody>
<tr>
<td>$T$ Temperature</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>$R_a$ Ohmic Alloy Sheet Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>$R_c$ Ohmic Contact Resistance</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>$a$ MESFET channel depth†</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>$N_d$ Nominal Doping Level</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>$d_s$ Ohmic Contact to Diode Metal Spacing</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>$d_e$ MESFET gate-drain and gate-source spacing</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

† Initial channel depth extremes are calculated from the pinch-off voltage variation and then the pinch-off variation used is recalculated from the extremes of channel depth and doping.

Device Model Parameters

Process Parameters Formulas

Density of Conduction State

The default value for the density of conduction states is given by

$$N_c = 4.7 \times 10^{17} \left( \frac{T}{300} \right)^{3/2} \text{[cm}^{-3}\text{]}.$$  

Low Field Drift Mobility

In the GaAs crystal the drift velocity at low electric field is proportional to electric field strength and decreases with higher impurity concentration because of scattering effects. The empirical relation used for low field
mobility is
\[ \mu = \frac{5.80521 \times 10^8}{T} N_d^{0.151} \text{[cm}^2/\text{V/s}]. \]

This is a good fit to experimental data [Hilsum and Rose-Innes 1961] for doping concentrations between $10^{15}$ and $10^{19}$ cm$^{-3}$.

**Saturation Velocity**

The electric field dependence of electron velocity displays negative differential property and eventual velocity saturation at high fields. This is due to the two valley band structure which has an increased effective mass in the higher valley. The empirical formula used by GaAsSPICE for the saturated velocity of electrons in a high electric field is
\[ v_s = 6000000 + 600 \mu - 0.02 \mu^2 \text{[cm/s]}. \]

This, the maximum electric field, and the maximum velocity equations are from [Shur 1987].

**Maximum Velocity Field**

Maximum electron velocity occurs at an electric field strength given by
\[ E_m = \frac{v_s}{\mu} \left[ 1.015 + 0.39 \left( 0.6 e^{(2 \times 10^{-3} \mu)} + 0.01 \right)^{-1/3} \right] \text{[V/cm]} \]

This is an empirical fit to the electron velocity formula given below.

**Maximum Electron Velocity**

Maximum electron velocity is given by
\[ v_m = v_s \left[ 1 + \frac{E_m \mu/v_s - 1}{1 + (0.6 e^{(2 \times 10^{-3} \mu)} + 0.01) (E_m \mu/v_s)^4} \right] \text{[V/cm]} \]

This is a simplified empirical formula given by Shur [1987].

**Schottky Barrier Height**

At the surface of GaAs, the existence of extra energy states in the energy gap affect electron affinity. The resulting affect on the Schottky barrier height is given by $\phi_b = c_1 \phi_m + c_2 \cdot \Delta \phi$ where $\phi_m$ is the work function of the metal. If $c_1 \to 0$ the Fermi level in the GaAs is tied to that of the surface states. This occurs when there is a high density of surface states and they can be filled in preference to transferring charge to the metal. On the other hand if $c_1 \to 1$ the barrier is not affected by surface states and is simply the difference between the metal work function and the GaAs electron affinity. Measured data [Sze 1965] for GaAs gives $c_1 = 0.07 \pm 0.05$, $c_2 = 0.49 \pm 0.24$ V.

The barrier is also affected by the doping level which varies the position of the Fermi level so the barrier height becomes $\phi_b = \phi_b^N_d^{N_c} + kT/q \ln \left( \frac{N_d}{N_c} \right)$. This can be compared with an empirical formula [Fukui 1979] for aluminium, $\phi_b = 0.026 \ln(N_d) - 0.25$ [eV] where $N_d$ is the doping concentration in carriers per cm$^3$.

The formula used here is
\[ \phi_b = c_1 \phi_m + c_2 + 8.617 \times 10^{-5} T \ln \left( \frac{N_d}{N_c} \right) \text{[eV]}. \]
Schottky Metal Work Function and Relative Electron Mass

The properties of the Schottky metal, used for diodes and gates, are required to define the characteristics of these junctions. The Metal work function, $\phi_m$, and the relative electron mass are required. For Aluminium, $\phi_m = 3.38$ [ITT 1975]. The effective mass of an electron is estimated to be 1.2.

Device Dimensions

Electrode Dimensions

The main dimensions are the lengths of the source, drain and gate and the spacing between these electrodes. The gate-length and electrode spacing are usually set to the smallest achievable with the process used.

Ohmic Contact Transfer Length

The transfer length of the epi-layer contact is given by $L_t = \sqrt{\frac{R_c}{R_a}}$ [Marlow and Das 1982]. This is a fundamental property of the contact used to calculate its resistance.

Channel Depth

The channel depth required to give the specified pinch-off voltage is

$$a = \sqrt{\frac{1.1047 \times 10^{-22}(\phi_b - V_{to})\varepsilon_r}{N_d}}$$

[Å]

Recommended Diode Length

The diode length, $L_c$, is a recommended quantity. It is chosen so that the diode will remain exponential up to the velocity saturation limited current that can be carried by the device.

A transmission line model can be used to determine the effect of edge conduction on diode current. Consider an infinitesimal diode element of length $dx$ contributing a current $di$. If the voltage of the anode (Schottky metal) of this diode is $V$ the voltage at the cathode is

$$v(x) = V - \frac{NkT}{q} \ln \left( \frac{di(x)}{dx} \frac{1}{i(x)} \right)$$

and the incremental change in cathode voltage is proportional to the epi-layer resistance under the diode metal:

$$\frac{dv(x)}{dx} = r_s \frac{i(x)}{2}$$

The solution to this system of differential equations has the form $i(x) = A \frac{e^{Bx+1}}{Bx+1}$.

Rearranging this equation gives the total voltage drop for the diode:

$$V = \frac{NkT}{q} \ln \left( \frac{I}{I_s} \right) + \frac{NkT}{q} \ln \left( \frac{I}{I_d} \right) + \frac{1}{2} + \frac{1}{4} \frac{I_d}{I} + 1$$

$$\approx \frac{NkT}{q} \ln \left( \frac{I}{I_s} \right) + \frac{NkT}{q} \ln \left( \frac{I}{I_d} + 1 \right)$$

The second logarithm is significant when $I$ is near or greater than $I_d$. That
is, the effect is significant when
\[ d_d \geq \frac{2NkTz}{IqP_a}. \]

The maximum current is limited to \( I_s=azqN_d\nu_m \) by velocity saturation. Also,
\[ r_s=\frac{1}{q\mu N_d} \], so the recommended contact length is set to \( L_c \geq \frac{2NkT\nu}{u_mq} \).

**Diode Model Parameters**

**Reverse Saturation Current**

Assuming a Maxwell velocity distribution and a barrier height many times \( q/kT \) above the Fermi level, the current density of electrons moving from the metal to the semiconductor is given by the Richardson-Dushman equation [Jay 1984].

In addition the barrier potential is reduced by the Schottky effect. For an electron moving into the semiconductor the barrier is a potential well formed by the positive charge left on the material surface and the imposed electric field \( E \). The barrier is lowered by \( \sqrt{\frac{qE}{4\pi\epsilon\epsilon'}} \) in a uniform field \( E \) [Sze 1985]. The formula used by GaAsSPICE is
\[
I_S = d_d \times 1.2 \times 10^6 \frac{m\mu m}{T^2} \exp\left(-\frac{q\Phi_0-0.012\sqrt{E_d/\epsilon'}}{kT}\right) \quad \text{[pA/\mu m]}
\]

**Emmission Coefficient**

At a neutral bias electrons are thermally emitted into the metal with a current density equivalent to \( I_D \approx A_s^* T^2 N_d N_c \). This is the Richardson-Dushman equation at junction bias equal and opposite to the barrier potential, \( V' = \Phi_0 \), with a weighting for the number of filled conduction states. \( A_s^* \) is the Richardson constant for the semiconductor.

The emission coefficient, \( N \), can be evaluated by fitting the SPICE equation to the points \( V' = \Phi_0 \), \( I_D = A_s^* T^2 \frac{N_d}{N_c} \) and \( V' = -\infty \), \( I_D = I_S \). The equation used is
\[
N = \frac{q\Phi_0-0.012\sqrt{E_d/\epsilon'}}{kT}\left[\ln\left(\frac{m^{*}N}{m\mu N_c} N_d \exp\left(\frac{q\Phi_0}{kT}\right)\right)^{-1}\right]^{-1}
\]

**Series Resistance**

The series resistance is composed of the ohmic contact resistance and the resistance of the epi-layer separating the ohmic and Schottky contacts. Note that the ohmic contact resistance increases as a hyperbolic cotangent when the contact length is less than the transfer length.

The thickness of the separating epi-layer is assumed to be the mean of its unetched thickness and the MESFET channel depth. The epi-layer thickness is reduced by the surface state depletion potential so its thickness
is determined from the epi-layer sheet resistance. The equation used is

\[ RS = \frac{R_c}{L_t} \coth \left( \frac{d_0}{L_t} \right) + \frac{d_s}{\mu q N_d} \left( \frac{a}{2 \times 10^8} - \frac{3.125 \times 10^{22}}{R_\alpha \mu N_d} \right)^{-1} \]  \[ \text{[\(\Omega \cdot \mu \text{m}\)].} \]

**Junction Capacitance**

The usual expression for junction capacitance, derived with the Gauss law, gives

\[ C_{JO} = d_d \times 8.422 \times 10^{-10} \sqrt{\frac{N_d \varepsilon_r}{\phi_b}} \]  \[ \text{[fF/\(\mu\text{m}\)].} \]

**Breakdown Voltage**

The breakdown voltage, BV, is set to the minimum of the avalanche or tunnelling potentials. Abrupt junction avalanche breakdown voltage is \(2.81 \times 10^{18} N_d^{-3/4}\) [Sze 1985]. The equation here, with correction for units is

\[ \text{BV} = \text{Minimum of } \frac{2eE_b^2}{qN_d} - \phi_b \text{ and } 8.886 \times 10^{13} N_d^{-3/4} \]  \[ \text{[V].} \]

**Junction Potential**

The diode junction potential, VJ, is set to the Schottky Barrier Height \(\phi_b\)

**Diode Parasitic Capacitance**

The physical capacitance between the Schottky and ohmic metals is calculated using an improved form of van Tuyl’s [1980] method. The coplanar capacitance, \(C_c\) [fF/\(\mu\text{m}\)], between the two conductors with length, \(d_d\) and \(d_o\), separated by a distance, \(d_s\) is

\[ C_c \approx \begin{cases} 3.13 \times 10^{-3} (\varepsilon_r + 1) N_d \frac{1.46}{1 - k'} & k' \geq 0.5 \\ 2.50 \times 10^{-2} (\varepsilon_r + 1) N_d \ln \frac{8.46}{k'} & k' < 0.5 \end{cases} \]

where \(k = \frac{d_d d_o}{(d_d + d_s)(d_o + d_s)}\)

The capacitance should be placed in parallel with the diode model.

**MESFET Model Parameters**

**Threshold Voltage**

Threshold Voltage, VTO, is set to the pinch-off voltage specified by the user.

**Transconductance Parameter**

The transconductance parameter is given in the Shockley expression as [van der Ziel 1976]

\[ \beta = \frac{q \mu N_d \alpha}{3 L W_\infty}. \]  \[ \text{[\(\mu\text{A/\(\mu\text{m/V})^2\).} \]

With the Statz model the 3 in the denominator becomes a 2 because a square law is used.
Saturation Parameter (JFET Model)

The saturation parameter is the ratio

$$\xi = \frac{v_m L \times 10^{-4}}{\mu (\phi_b - V_{to})}.$$ 

Doping Tail Extending Parameter (Statz Model)

The doping tail extending parameter, $b$, is set to match the saturation current:

$$\frac{\beta (\phi_b - V_{to})^2}{1 + b (\phi_b - V_{to})} = v_m q N_d a \left( 1 - \sqrt{\frac{\xi}{\xi + 1}} \right) L$$

The saturated portion of the channel continues to increase with increasing drain-source potential as described by Pucel et al. [1975]. The length of the saturated portion increases rapidly with drain-source potential until it reaches $L_{sat}$ when $\frac{V_{ds}}{(\phi_b - V_{to})} = \text{Error}$. When the drain-source potential is greater than this empirical condition the change in saturated region length is not so rapid and is considered to be channel length modulation.

$$L_{sat} = \frac{2a}{\pi} \ln \left( \frac{\pi L}{2a (\xi + 1)} + \sqrt{\left( \frac{\pi L}{2a (\xi + 1)} \right)^2 + 1} \right)$$

Saturation Parameter (Statz Model)

The saturation parameter, $\alpha$, is chosen so that

$$\frac{\partial I_{ds}}{\partial V_{ds}} = q \mu N_d \frac{a}{L} \text{ at } V_{gs} = \phi_b$$

and $V_{ds} = 0$:

$$\frac{\alpha \beta (\phi_b - V_{to})^2}{1 + b (\phi_b - V_{to})} = q \mu N_d \frac{a}{L}$$

Channel-Length Modulation Parameter

The length of the saturated portion of the channel, $\Delta L$, is

$$\Delta L = \frac{2a}{\pi} \ln \left( \frac{\pi (V_{ds} - V_{sat}) L}{2 \xi a W_{oo}} + \sqrt{\left( \frac{\pi (V_{ds} - V_{sat}) L}{2 \xi a W_{oo}} \right)^2 + 1} \right)$$

The current through the unsaturated portion of the channel is inversely proportional to its length so the transconductance parameter, $\beta$, is increased by $\frac{L}{L - \Delta L}$ which is modelled by the factor $(1 + \lambda V_{ds})$.

$$\frac{L}{L - \Delta L} = (1 + \lambda V_{ds})$$

A problem exists with this expression because $\lambda$ is a function of $V_{ds}$. However, the function is slow changing and a reasonable value can be obtained by setting $V_{ds} = 3 W_{oo}$. The saturation potential, $V_{sat} = \frac{\xi}{\xi + 1} W_{oo}$.

Drain Feedback Parameter

Hartgring [1982] presented an expression for the effective drain feedback capacitance from which the drain feedback parameter can be determined.

$$C_{dfb} = z C_{dfb} V_{ds}^{-1/2} \ln(L/L_o)$$

The change in channel charge density is
\[ \Delta qN = \frac{C_{\text{dh}}V_{\text{ds}}}{azL} \]

This charge causes a change in depletion potential modelled by \( \eta V_{\text{ds}} \). The change in depletion potential is

\[ \Delta V_{\text{to}} = \frac{q\Delta N \varepsilon^2}{2\varepsilon} = \frac{C_{\text{dh}}\alpha V_{\text{ds}}}{2\varepsilon\varepsilon L} \]

\[ \eta = \frac{aC_{\text{dh}}\ln(L/L_o)}{4\varepsilon L\sqrt{W_\infty}} \]

where \( C_{\text{dfbo}} = 1.87 \times 10^{-12} \text{ F/cm}^{1.5} \) and \( L_o = 1.7 \times 10^{-5} \text{ cm} \) are empirical constants.

**Velocity Reduction Parameter**

The velocity reduction parameters model the reduction in drain current due to the reduction in electron velocity with increasing electric field. The electron velocity reduces from its maximum velocity to the saturated velocity and the parameter \( \kappa \) sets to the extent of this reduction.

\[ \kappa = 1 - \frac{v_e}{v_m} \]

**Source and Drain Ohmic Resistance**

The series resistance is composed of the ohmic contact resistance and the resistance of the epi-layer separating the ohmic and Schottky contacts. Note that the ohmic contact resistance increases as a hyperbolic cotangent when the contact length is less than the transfer length.

The thickness of the separating epi-layer is assumed to be the mean of its unetched thickness and the MESFET channel depth. The epi-layer thickness is reduced by the surface state depletion potential so its thickness is determined from the epi-layer sheet resistance.

The equation used for both the Source and Drain resistance is

\[ RS = R_c \left( \frac{d_o}{L_t} \coth \left( \frac{d_o}{L_t} \right) \right) + \frac{d_g}{\mu q N_d} \left( \frac{a}{2 \times 10^8} - \frac{3.125 \times 10^{22}}{R_d \mu N_d} \right) \]

[Ω·μm].

**Gate-Source Junction Capacitance**

Adding a fringe component to the usual expression for junction capacitance, derived with the Gauss law, gives

\[ CGS = 8.422 \times 10^{-10} L \sqrt{\frac{N_d \varepsilon}{\varepsilon_b}} + 0.01391 \varepsilon_r \]

[fF/μm].

**Gate-Drain Junction Capacitance**

The gate-drain junction capacitance is merely the result of the geometry of the FET [Takada 1982]

\[ CGD = 0.00556 \varepsilon_r \]

[ff].

**Gate Junction Potential**

The junction potential is set to the barrier height \( \phi_b \).
Gate Junction Reverse Leakage Current

This is the diode reverse current scaled for the gate length.

\[ IS = \frac{L}{d_d} IS \]

**MESFET Parasitic Capacitance**

The physical capacitance between the MESFET electrodes is calculated using an improved form of van Tuyl’s [1980] method in the same way as the diode parasitic is determined.

**Not calculated and unsupported parameters**

Transit Time

At high fields minority carrier (hole) injection occurs with a minority carrier storage time, \( \tau_b \), typically less than \( 10^{-15} \) s in GaAs. This is negligibly small so that the diode model parameter TT can be left at the default zero value.

Grading Coefficient

The diode model grading coefficient, M, is left at the default value, 0.5.

Energy Gap

The diode model energy gap parameter is used for the temperature modelling which is not supported by GaAsSPICE or SPICE version 3. If required it should be set to

\[ N \times \left( \phi_b - 0.012 \sqrt{E_h/e_r} \right) \] [eV].

Saturated-Current Temperature Exponent

The diode model Saturated-Current Temperature exponent, XTI, is used for temperature modelling of IS and is set to 2\( \times N \).

Noise Parameters

Noise analysis is not supported.

Capacitance Coefficient

The capacitance fudge coefficient, FC, is left at the default value of 0.5.

**Gate Design Procedure**

**Device Characteristics**

The design of logic gates is simplified by using a linearized MESFET model which is characterised by straight line segments. A single model is sufficient because all devices in the depletion mode circuit differ only in width. The model uses six parameters to define the device characteristics for a one unit wide device. The zero-gate-bias saturated current, \( I_{ds} \), the transconductance, \( g_m \), the near-pinch-off transconductance, \( g_x \), and the effective near-pinch-off zero-gate-bias saturated current, \( I_x \), define the
relation between the saturated current and the gate-source bias. The drain-source potential of the saturation knee is defined by the effective zero-current saturation potential, \(V_s\), and the conductance of saturation potential, \(G_s\).

**Design Equations**

Consider the inverter stage in BFL driven by high and low logic levels, \(V_h\) and \(V_l\), respectively. The corresponding potentials at the output of an inverting logic gate, which are the same as those applied to the input of the next logic gate, can be evaluated in terms of the voltage drops over the devices in the gate. A logic high output is set by the positive power supply potential, \(V_{dd}\), less the potential drop over the source follower and diode chain, \(V_{ds\,sf} + V_d\). The output logic threshold, \(V_{mid}\), occurs when the switch transistor and pull-up draw the same current and the node between them is at half the supply potential. The logic low at the output is nominally the potential over the switch device shifted by the diode chain but can be limited by the negative supply potential through the pull-down transistor. The gate-source potential of the source follower is assumed to be zero.

First, starting with an initial required logic swing, \(V_h - V_l\), the values of the drain-source potentials of the devices are estimated using the equations which follow with \(V_h\) set to \(\Phi_b/2\).

Second, these estimates are used to determine the necessary power rails and diode chain potential. The power supply values can be rounded to a nominal value.

\[
V_{ss} \leq V_{ds\,sf} - V_{ds\,pd} - V_d
\]

\[
V_{dd} = V_h - V_l + V_{ds\,sf} + V_{ds\,sw}
\]

\[
V_d \geq V_{dd} - V_{ds\,sf} - \Phi_b/2
\]

Third, the following equations are solved iteratively to give a self consistent solution for the logic levels.

\[
V_h = V_{dd} - V_{ds\,sf} - V_d
\]

\[
V_l = \max \{ \frac{z_{pu}}{z_{sw}} I_{ds} - V_d, V_{ss} + V_{ds\,pd} \}
\]

\[
V_{ds\,sw} = \frac{z_{pu}}{z_{sw}} I_{ds} + g_m V_h \left( \frac{I_{ds} + g_m V_h + V_s}{G_s + G_s} \right)
\]

\[
V_{ds\,pd} = \frac{I_{ds}}{G_s} + V_s
\]

\[
V_{ds\,pu} = \frac{z_{sw}}{z_{pu}} \left( \frac{I_{ds}}{G_s} + V_s \right) \max \{ 0, I_s + g_m V_l, I_{ds} + g_m V_l \}
\]
It can be assumed the widths of the pull-up transistor and the source follower are the same.

Fan-In and Fan-Out Loading

If there are $f_{in}$ switch transistors in the inverter stage one of them can switch the gate when the others are off. The width of the pull-up transistor must be extended to offset the fan-in loading current through the off switches.

$$z_{pu \ total} = z_{pu} + (f_{in} - 1)z_{sw}(I_s + g_m V_i)$$

Dual-Gate Switches

The width of the dual-gate switch transistor, $z_{an}$, must be set so that it can deliver the same current as a single-gate device. Dual-gate transistors are modelled as two series single-gate devices. The upper gate has the voltage drop of the lower device added to its gate-source junction potential. The average of the thresholds for the two gates of the dual-gate transistor is set to the threshold of the single-gate transistor.

$$\frac{z_{an}}{z_{pu}} = \frac{2 + g_m / G_s}{2 + (V_s - V_h - V_l) / V_p}$$

Diode Chain Specification

The width and hence number of diodes is set so that the change in diode potential drop caused by process changes of resistance is approximately the same as the change over the expected operating temperature range. The following implicit equation is used to satisfy this condition for the current supplied by the pull-down transistor.

$$\frac{z_{pd} I_{dss} R_s}{z_d} = \frac{n k T}{q} \ln \left( \frac{z_{pd} I_{dss}}{z_d I_s} \right)$$

The number of diodes necessary to give the required voltage drop is calculated to the nearest integer.

$$\eta = \frac{V_d}{\frac{n k T}{q} \ln \left( \frac{z_{pd} I_{dss}}{z_d I_s} \right) + \frac{z_d I_{dss} R_s}{z_d}}$$

With the number of diodes known, the width of the diodes can be set to give the correct voltage drop.

**AC Optimization**

It still remains to define the relative size of the level shift devices to that of the
inverter stage. This relation determines the fan-out capability of the gate and can be optimised for maximum speed.

The optimum ratio of transistor widths for minimum fall-time occurs when the Setting $z_{pd} = z_{sf}$ gives final expressions for the rise- and fall-times of the gate.

$$\frac{z_{sf}}{z_{sw}} = (V_h - V_l) \sqrt{\frac{F}{2A_{\text{th}} V_{po}}}$$

### Process Variations

The operation of the gate design including operation of dual-gate inputs must be checked at the extremes of process variations. The logic level calculation procedure illustrated below determines the extremes of logic and threshold levels for all combinations of variations of the parameters (temperature, parasitic resistance, doping level, channel depth and electrode spacing). The boxes in the diagram represent four identical sets of logic gates driven by the same input level. The extreme of one logic level at the input produces, in the worst case, the extreme of the complementary level. The design is robust against process variation if the worst case logic high is above the highest threshold level and the worst case logic low is below the lowest threshold level. Note however that the noise margin is reduced when the logic levels are close to the threshold level. It is assumed that all the devices in a single logic gate have the same parameters.

Each gate in the set has linearized MESFET and diode parameters corresponding to one of the combinations of parameter variations. For each gate the input logic level and the linearized models are used in the design equations to determine the output logic levels.
References


9.4 SPICE Modifications

The modifications required to implement the new JFET model described in Chapter 3 have been set out in the text file reproduced in the following pages. This gives all the necessary changes.
This file contains the modifications necessary to implement the Sydney University enhanced JFET model in SPICE 3b1. This model is designed to simulate accurately both GaAs MESFETs and JFETs. It universally handles any gate length by allowing the user to adjust the drain current saturation.

The source code files to be changed are: (note that some existing code is listed to help position the modifications in each file)

1. Documentation
2. JFET.c
3. JFETacLoad.c
4. JFETdefs.h
5. JFETmAsk.c
6. JFETmParam.c
7. JFETpzLoad.c
8. JFETsetup.c
9. JFETload.c
The SPICE JFET model has been enhanced so that short and medium channel length devices and GaAs MESFETs can be simulated. It can be understood as being multi-level in a similar manner as the MOS models.

The simplest form, or lowest level, is identical to the original JFET model derived from the FET model of Shichmann and Hodges. The dc characteristics are defined by the parameters VTO and BETA, which determine the variation of drain current with gate voltage, LAMBDA, which determines the output conductance, and IS, the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. This form is automatically present when the additional parameters are not specified or set to default values.

In the second level of understanding, the model has an improvement which is activated by setting the doping profile parameter, B, to other than unity. The model describes drain current in the linear mode as

\[
I_{ds} = \text{BETA} \cdot V_{gs} \cdot \left( B \cdot \left( 2 \cdot (V_{gs} - V_{TO}) - V_{gs} \right) + \frac{2}{B-1} \cdot \left( V_{gs} + 3 \cdot (V_{gs} - V_{TO}) \cdot (V_{gs} - V_{TO} - V_{ds}) \right) \right)
\]

and when B is set to 0.6, it very closely follows the standard van der Ziel [1] FET equation which has the form

\[
I_{ds} \propto d_s - s^2 - \frac{d_s}{3}
\]

where s and d are the extents of channel depletion at the source and drain ends of the channel.

In the next form of the model, the short channel effects of drain-induced barrier lowering and electron velocity saturation are present. Barrier lowering is set by the drain feedback parameter, ETA, which is similar to the same parameter in the BSIM (MOS level 4) model. The high frequency drain feedback parameter, ZETA, is added to ETA when rates of drain potential change are greater than the drain feedback time constant, TAU. This is used to simulate the change in drain conductance as a function of frequency which is observed in GaAs devices. Velocity saturation is set by the saturation parameter, XI. This parameter specifies the drain to source potential, Vsat, at which drain current saturation occurs.

\[
V_{sat} = \frac{\text{XI} \cdot (PB-VTO) \cdot (V_{gs} - V_{TO})}{\text{XI} \cdot (PB-VTO) + (V_{gs} - V_{TO})}
\]

This allows the simulation of short channel devices where drain current saturation due to electron velocity limiting occurs at a lower drain to source potential than pinch-off saturation. The saturation parameter, XI, has the same interpretation as the one used in the model proposed by Pucel et al. [2]. The saturation occurs smoothly, using a fourth order polynomial expression, in a manner which closely fits that predicted by the Pucel et al. model.

The most complex form of the model includes the effect of electron velocity reduction present in GaAs devices. The effect is observed as a reduction of drain current with increasing drain potential due to the Gunn domain near the drain. The reduction is adjusted with two parameters: KAPPA, which determines the extent of the reduction (zero is no reduction), and THETA which determines the range of drain...
to source potential, in multiples of the saturation potential, \( V_{sat} \), over which the reduction occurs.

Charge storage is modelled by one of two methods as selected by the CMOD parameter. When CMOD=1 (default), the original model is used with nonlinear depletion layer capacitances for both gate junctions which vary as the \(-1/2\) power of junction voltage and are defined by the parameters CGS, CGD and PB. When CMOD=2, the capacitance model becomes the one based on the GaAs FET model of Statz et al. [3]. The capacitance pinch-off parameter, \( X_C \), allows the user to specify the amount that capacitance reduces as the junction bias depletes the channel in the Statz model. If \( X_C = 1 \), there is no reduction in capacitance.

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/* JFET.c ***************************************************/
/*
* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added May 1988 Anthony E. Parker
*/

IOP("pjf", JFET_MOD_PJF, IF_FLAG,"P type JFET model"),
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
IOP("b", JFET_MOD_B, IF_REAL,"Doping tail parameter"),
IOP("xi", JFET_MOD_XI, IF_REAL,"Drain Current saturation param."),
IOP("kappa", JFET_MOD_KAPPA, IF_REAL,"Sat. vel. reduction parameter"),
IOP("theta", JFET_MOD_THETA, IF_REAL,"Sat. vel. reduc. rate parameter"),
IOP("cmod", JFET_MOD_CAPMODEL, IF_REAL,"Capacitance model"),
IOP("xc", JFET_MOD_XC, IF_REAL,"Capaitance pinch-off reduction"),
IOP("eta", JFET_MOD_ETA, IF_REAL,"Drain feedback parameter"),
IOP("zeta", JFET_MOD_ZETA, IF_REAL,"Hi. Freq. Drain feedback param."),
IOP("tau", JFET_MOD_TR, IF_REAL,"Drain feedback relaxation time"),
/* end Sydney University mod. */

/* JFETacLoad.c ***************************************************/
/*
* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added May 1988 Anthony E. Parker
*/

double xgd;
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
double gfbds;
double xfbd;
double wt;
/* end Sydney University mod. */

xgd = *(ckt->CKTstate0 + here->JFETqgd) * ckt->CKTomega;
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/

wt = model->JFETtau * ckt->CKTomega;
xfbd = model->JFETeta * gm * wt / (1 + wt * wt);
gfbds = xfbd * wt;
*(here->JFETdrainPrimeDrainPrimePtr ) += gfbds;
*(here->JFETdrainPrimeDrainPrimePtr +1) += xfbd;
*(here->JFETsourcePrimeSourcePrimePtr ) += gfbds;
*(here->JFETsourcePrimeSourcePrimePtr +1) += xfbd;
*(here->JFETdrainPrimeSourcePrimePtr ) += (-gfbds);
*(here->JFETdrainPrimeSourcePrimePtr +1) += (-xfbd);
*(here->JFETsourcePrimeDrainPrimePtr ) -= gfbds;
*(here->JFETsourcePrimeDrainPrimePtr +1) -= xfbd;
/* end Sydney University mod. */
/* JFETdefs.h *******************************************************/
/* *
* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added May 1988 Anthony E. Parker
*/
#define JFETcqgd JFETstate+12
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
#define JFETvdsfB JFETstate+13
/* end Sydney University mod. */

double JFETvcrit;
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
double JFETxi;         /* velocity saturation index */
double JFETb;          /* doping tail parameter */
double JFETteta;       /* drain feedback parameter */
double JFETtetaT;      /* high frequency drain feedback parameter */
double JFETtheta;      /* rate of saturation vel. reduction parameter */
double JFETkappa;      /* extent of vel. reduction parameter */
double JFETxc;         /* proportion of capacitance reduction at pinch-off */
double JFETcapModel;   /* select capacitance model to use */
double JFETtau;        /* relaxation time for drain feedback */
double JFETbFac;
double JFETXiWoo;
/* end Sydney University mod. */

unsigned JFETdepletionCapCoeffGiven : 1;
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
unsigned JFETxiGiven : 1;
unsigned JFETtetaGiven : 1;
unsigned JFETtetaTGiven : 1;
unsigned JFETbGiven : 1;
unsigned JFETthetaGiven : 1;
unsigned JFETkappaGiven : 1;
unsigned JFETxcGiven : 1;
unsigned JFETcapModelGiven : 1;
unsigned JFETtauGiven : 1;
/* end Sydney University mod. */

#define JFET_MOD_PJF 112
/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/
#define JFET_MOD_B 150
#define JFET_MOD_CAPMODEL 151
#define JFET_MOD_XC 152
#define JFET_MOD_Eta 153
#define JFET_MOD_Kappa 154
#define JFET_MOD_Theta 155
#define JFET_MOD_TR 156
#define JFET_MOD_Xi 157
#define JFET_MOD_Zeta 158
/* end Sydney University mod. */
case JFET_MOD_VCRIT:
    value->rValue = here->JFETvcrit;
    return(OK);

// Modification for Sydney University Universal JFET model
// Copyright (c) May 1988 Anthony E. Parker
// Laboratory for Communication Science Engineering
// Sydney University Department of Electrical Engineering
/

case JFET_MOD_B:
    value->rValue = here->JFETb;
    return(OK);

case JFET_MOD_CAPMODEL:
    value->rValue = here->JFETcapModel;
    return(OK);

case JFET_MOD_XC:
    value->rValue = here->JFETxc;
    return(OK);

case JFET_MOD_ETA:
    value->rValue = here->JFETeta;
    return(OK);

case JFET_MOD_ZETA:
    value->rValue = here->JFETzeta;
    return(OK);

case JFET_MOD_KAPPA:
    value->rValue = here->JFETkappa;
    return(OK);

case JFET_MOD_THETA:
    value->rValue = here->JFETtheta;
    return(OK);

case JFET_MOD_TR:
    value->rValue = here->JFETtau;
    return(OK);

case JFET_MOD_XI:
    value->rValue = here->JFETxi;
    return(OK);

/* end Sydney University mod. */

/* JFETmParam.c **************************************************************/
/*
* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added May 1988 Anthony E. Parker
* /

// Modification for Sydney University Universal JFET model
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// Laboratory for Communication Science Engineering
// Sydney University Department of Electrical Engineering
*/

case JFET_MOD_PJF:
    mods->JFETtype = PJF;
    break;

// Modification for Sydney University Universal JFET model
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// Laboratory for Communication Science Engineering
// Sydney University Department of Electrical Engineering
*/

case JFET_MOD_ETA:
    mods->JFETetaGiven = TRUE;
    mods->JFETeta = value->rValue;
    break;

case JFET_MOD_ZETA:
    mods->JFETzetaGiven = TRUE;
    mods->JFETzeta = value->rValue;
    break;

case JFET_MOD_XI:
    mods->JFETxiGiven = TRUE;
    mods->JFETxi = value->rValue;
    break;
case JFET_MOD_XC:
    mods->JFETxc = value->rValue;
    mods->JFETxcGiven = TRUE;
    break;
case JFET_MOD_CAPMODEL:
    mods->JFETcapModel = value->rValue;
    mods->JFETcapModelGiven = TRUE;
    break;
case JFET_MOD_THETA:
    mods->JFETtheta = value->rValue;
    mods->JFETthetaGiven = TRUE;
    break;
case JFET_MOD_KAPPA:
    mods->JFETkappa = value->rValue;
    mods->JFETkappaGiven = TRUE;
    break;
case JFET_MOD_B:
    mods->JFETb = value->rValue;
    mods->JFETbGiven = TRUE;
    break;
case JFET_MOD_TR:
    mods->JFETtau = value->rValue;
    mods->JFETtauGiven = TRUE;
    break;
/* end Sydney University mod. */

/* JFETpzLoad.c **************************************************************/
/* Copyright (c) 1985 Thomas L. Quarles
 * Sydney University Universal JFET model added May 1988 Anthony E. Parker */

double xgd;
/* Modification for Sydney University Universal JFET model
 * Copyright (c) May 1988 Anthony E. Parker
 * Laboratory for Communication Science Engineering
 * Sydney University Department of Electrical Engineering */

double gfbds;
double xfbds;
double wt;
/* end Sydney University mod. */

xgd = *(ckt->CKTstate0 + here->JFETqgd);
/* Modification for Sydney University Universal JFET model
 * Copyright (c) May 1988 Anthony E. Parker
 * Laboratory for Communication Science Engineering
 * Sydney University Department of Electrical Engineering */

wt = model->JFETtau;
xfbds = model->JFETtauPrime
    * (1 + wt*s->real)*s->imag - wt*s->real*s->imag)
        / ((1+s->real*wt)*(1+s->real*wt) + (s->imag*wt)*(s->imag*wt));
    /* end Sydney University mod. */
if(model->JFETsourceResist != 0) {
    model->JFETsourceConduct = 1/model->JFETsourceResist;
} else {
    model->JFETsourceConduct = 0;
}

if(!model->JFETxiGiven) {
    model->JFETxi = 10000;
}
if(!model->JFETetaGiven) {
    model->JFETeta = 0;
}
if(!model->JFETzetaGiven) {
    model->JFETzeta = 0;
}
if(!model->JFETthetaGiven) {
    model->JFETtheta = 3;
}
if(!model->JFETkappaGiven) {
    model->JFETkappa = 0;
}
if(!model->JFETcapModelGiven) {
    model->JFETcapModel = 1;
}
if(!model->JFETxcGiven) {
    model->JFETxc = 0.0;
}
if(!model->JFETbGiven) {
    model->JFETb = 1.0;
}
if(!model->JFETtauGiven) {
    model->JFETtau = 0.0;
}

model->JFETXiWoo = 1/model->JFETxi/(model->JFETgatePotential - model->JFETthreshold);
model->JFETbFac = (1 - model->JFETb)/(model->JFETgatePotential - model->JFETthreshold);

/* end Sydney University mod. */

/* Modification for Sydney University Universal JFET model
* Copyright (c) May 1988 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering */

/* JFETsetup.c ********************************************* */

/* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added May 1988 Anthony E. Parker */
```c
/* JFETload.c****************************************************************/
/*
* Copyright (c) 1985 Thomas L. Quarles
* Sydney University Universal JFET model added January 1989 Anthony E. Parker
*/

double sarg;
/*  Modification for Sydney University Universal JFET model
*  Copyright (c) May 1988 Anthony E. Parker
*  Laboratory for Communication Science Engineering
*  Sydney University Department of Electrical Engineering
*/
*  double twob; */

double DrainFeedback;
double SatParm,TranParm;
double eta;
double xi;
double phib,vto,Vs,VsVg;
double apart,bpart,cpart;
double K;
double Bfac;
double theta,sqThetaK;
double cgdna,cgdnb,cgdnc,cgdnd;
double cgsna,cgsnb,cgsnc,cgsnd;
double qgga,qggb,qggc,qggd;
double qggnew();
double vgd1,vgs1;
double vcap2;
double xc;
double vmax;
/*  end Sydney University mod. */

cg = cg+cgd;
/* Modification for Sydney University Universal JFET model
* Copyright (c) January 1989 Anthony E. Parker
* Laboratory for Communication Science Engineering
* Sydney University Department of Electrical Engineering
*/

if( ckt->CKTmode & MODETRAN ) {
    if( ckt->CKTmode & MODEINITTRAN ) {
        *(ckt->CKTstate1 + here->JFETvdsfb) = vds ;
    }
    DrainFeedback = 4/(4 + ckt->CKTdelta/model->JFETtau) ;
    DrainFeedback = DrainFeedback * DrainFeedback * DrainFeedback
    * DrainFeedback * DrainFeedback
    *(ckt->CKTstate0 + here->JFETvdsfb) = vds - DrainFeedback ;
} else {
    DrainFeedback = 0;
}

eta = model->JFETeta;
Vto = model->JFETthreshold;
if (vds >= 0) {
    vgst = vgs + eta * vds - vto + model->JFETzeta * DrainFeedback ;
    /*
    * compute drain current and derivatives for normal mode
    */
    if (vgst <= 0) { /*
        * normal mode, cutoff region
        */
        cdrain = 0;
        gm = 0;
        gds = 0;
    } else {
        betap = beta*(1 + model->JFETlModulation*vds);
        Bfac = model->JFETbFac;
        VsVg = 1/(1 + vgst*model->JFETXiWoo);
        K = 1 - vds/VsVg/vgst;
        if (K >= 0) {
```
/ * normal mode, linear region */
apart = 2*model->JFETb + 3*Bfac*(vgst - vds);
cpart = vds*(vds*(Bfac*vds - model->JFETb)+vgst*apart);
cdrain = betap*cpart;
gm = betap*vds*(apart + 3*Bfac*vgst);
gds = betap*(vgs - vds)*apart + beta*model->JFET1Modulation*cpart + eta*gm;
} else {
  Bfac = vgst*Bfac;
  xi = model->JFETxi;
part = K*xi/VsVg + 1;
  TranParm = cpart*cpart*cpart;
  SatParm = (1 - VsVg)/(4*xi);
  Vs = vgst*VsVg;
apart = 2*model->JFETb + 3*Bfac*(1 - VsVg);
  gm = betap*Vs*(apart+3*Bfac + VsVg*(apart+3*Bfac*SatParm - VsVg*(apart - 3*(apart- Bfac*VsVg)*SatParm)));
  if (TranParm < 0) {
    /* normal mode, saturation region */
    cpart = Vs*(apart*(vgst+Vs*Sat Parm)-Vs*(model->JFETb-Bfac*VsVg));
cdrain = betap*cpart;
gds = model->JFET1 Modulation*beta*cpart + eta*gm;
  } else {
    /* normal mode, transition region */
    bpart = 0.75*Bfac*(K + VsVg*(4*SatParm - K));
part = Vs*(apart*vgst*(l + SatParm*(VsVg - Tran Parm*(K*xi+VsVg)) - Vs*(model->JFETb-Bfac*VsVg));
cdrain = betap*cpart;
    gm = gm + betap*Vs*Tran Parm*(apart*K + bpart
  + VsVg*(apart*(l-2.25*K)- VsVg*(apart*(l-1.25*K)
  + bpart - 3*(apart*Sat Parm))));
gds = model->JFET1Modulation*beta*cpart + eta*gm
  + apart*betap*vgst*(1 - VsVg)*Tran Parm;
  } K = vds*model->JFETXiWoo - 1;
  if (K*model->JFETkappa > 0) {
    /* normal mode, sat. velocity reduction routine */
    sqThetaK = model->JFETtheta / K;
    sqThetaK = sqThetaK * sqThetaK;
    SatParm = model->JFETkappa/(sqThetaK+1);
gm = gm*(1-SatParm);
gds = gds*(1-SatParm)
    -2*cdrain*SatParm*(l/K+1)/(l+1/sqThetaK)/vds;
cdrain = cdrain*(1 - Sat Parm);
  } else {
    vgd = vgd - eta * vds - vto - model->JFETzeta * DrainFeedback ;
    /* compute drain current and derivatives for inverse mode */
    if (vgdt <= 0) {
      /* inverse mode, cutoff region */
cdrain = 0;
gm = 0;
gds = 0;
    } else {

betap = beta*(1 - model->JFETlModulation*vds);
Bfac = model->JFETbFac;
VsVg = 1/(1 + vgdt*model->JFETXiWoo);
K = 1 + vds/VsVg/vgdt;
if (K >= 0) {
  /* inverse mode, linear region */
  apart = 2*model->JFETb + 3*Bfac*(vgdt + vds);
cpart = vds*(-Bfac*vds-model->JFETb)+vgdt*apart;
cdrain = betap*cpart;
gm = betap*vds*(apart + 3*Bfac*vgdt);
gds = betap*(vgdt + vds)*apart
     - beta*model->JFETlModulation*cpart - (eta+1)*gm;
} else {
  xi = model->JFETxi;
  Bfac = vgdt*Bfac;
cpart = K*xi/VsVg + 1;
  TranParm = cpart*cpart*cpart;
  SatParm = (1 - VsVg)/(4*xi);
  Vs = vgdt*VsVg;
apart = 2*model->JFETb + 3*Bfac*(1 - VsVg);
gm = -betap*Vs*(apart+3*Bfac+VsVg)(apart+3*Bfac*SatParm
     - VsVg)(apart - 3*(apart - Bfac*VsVg)*SatParm));
  if (TranParm < 0) {
    /* inverse mode, saturation region */
    cpart=Vs*(apart*(vgdt+Vs*SatParm)
     -Vs*(model->JFETb-Bfac*VsVg));
cdrain = - betap*cpart;
gds = model->JFETlModulation*beta*cpart-(eta+1)*gm;
  } else {
    /* inverse mode, transition region */
    bpart = 0.75*Bfac*(K + VsVg*(4*SatParm - K));
cpart = Vs*(apart*vgdt*(1 + SatParm)*(VsVg
     - TranParm*(K*xi+VsVg)))
     - Vs*(model->JFETb-Bfac*VsVg));
cdrain = - betap*cpart;
gm = gm + betap*Vs*TranParm*(apart*K + bpart
     + VsVg*(apart*(1-2.25*K)-VsVg*(apart*(1-1.25*K)
     + bpart - 3*apart*SatParm));
gds = model->JFETlModulation*beta*cpart-(eta+1)*gm
     + apart*betap*vgdt*(1 - VsVg)*TranParm;
}  
K = - vds*model->JFETXiWoo - 1;
if (K*model->JFETkappa > 0) {
  /* inverse mode, sat. velocity reduction routine */
sqThetaK = model->JFETtheta / K;
sqThetaK = sqThetaK * sqThetaK;
SatParm = model->JFETkappa/(sqThetaK+1);
gm = gm*(1-SatParm);
gds = gds*(1-SatParm)-2*cdrain*SatParm*
     (1/K+1/(1+1/sqThetaK))/vds;
cdrain = cdrain*(1-SatParm);
}  
}  
}  
}
/* The original section is now commented out by this ifdef */
#ifdef notdef
/* end Sydney University mod. */


/* end of deleted section */
#endif notdef
/* end Sydney University mod. */

/* compute equivalent drain current source */

 cd=cdrain-cgd;
 if ( (ckt->CKTmode & (MODETRAN | MODEAC | MODEINITMSIG) ) ||
 ( (ckt->CKTmode & MODETRANOP) && (ckt->CKTmode & MODEUIC)) ){
    /* charge storage elements */
    czgs=model->JFETcapGS*here->JFETarea;
    czgd=model->JFETcapGD*here->JFETarea;
    /* Modification for Sydney University Universal JFET model
    * Copyright (c) January 1989 Anthony E. Parker
    * Laboratory for Communication Science Engineering
    * Sydney University Department of Electrical Engineering */
    if ( model->JFETcapModel == 1 ) {
        /* standard JFET capacitance model */
        twop=model->JFETgatePotential+model->JFETgatePotential;
        fcpb2=model->JFETdepletionCap*model->JFETdepletionCap;
        czgsf2=czgs/model->JFETf2;
        czgdf2=czgd/model->JFETf2;
        if (vgs < model->JFETdepletionCap) {
            sarg=sqrt(1-vgs/model->JFETgatePotential);
            *(ckt->CKTstate0 + here->JFETqgs) = twop*czgs*(1-sarg);
            capgs = czgs/sarg;
        } else {
            *(ckt->CKTstate0 + here->JFETqgs) = czgs*model->JFETf1 +
            czgsf2*(model->JFETf3 *(vgs-
                model->JFETdepletionCap)+(vgs*vgs-fcpb2)/
                (twop+twop));
            capgs = czgsf2*(model->JFETf3+vgs/twop);
        }
        if (vgd < model->JFETdepletionCap) {
            sarg=sqrt(1-vgd/model->JFETgatePotential);
            *(ckt->CKTstate0 + here->JFETqgd) = twop*czgd*(1-sarg);
            capgd = czgd/sarg;
        } else {
            *(ckt->CKTstate0 + here->JFETqgd) = czgd*model->JFETf1+
            czgdf2*(model->JFETf3* (vgd-
                model->JFETdepletionCap)+(vgd*vgd-fcpb2)/
                (twop+twop));
            capgd = czgdf2*(model->JFETf3+vgd/twop);
        }
    } else {
        /* code for the Statz et. al. capacitance model
         * IEEE Tran Elec Dev Feb 87,
         * Modified at Sydney University */
        vcap2 = (0.5/(model->JFETXiWoo*(xi+1)));
        vcps = vcap2 * vcap2;
        vcps = model->JFETxc;
        vgs1 = *(ckt->CKTstate1 + here->JFETvgs);
        vgd1 = *(ckt->CKTstate1 + here->JFETvgd);
        vmax = model->JFETdepletionCap;
        phib = model->JFETgatePotential;
Appendix: SPICE Modifications

```
qgga = qggnew(vgs, vgd, phib, vcap2, vto, vmax, xc, czgs, czgd, &cgsna, &cgdna);
qggb = qggnew(vgs1, vgd, phib, vcap2, vto, vmax, xc, czgs, czgd, &cgsnb, &cgdnb);
qggc = qggnew(vgs, vgd1, phib, vcap2, vto, vmax, xc, czgs, czgd, &cgsnc, &cgdnnc);
qggd = qggnew(vgs1, vgd1, phib, vcap2, vto, vmax, xc, czgs, czgd, &cgsnd, &cgdnnd);
if (ckt->CKTmode & MODEINITTRAN) {
    *(ckt->CKTstate1 + here->JFETqgs) = qgga;
    *(ckt->CKTstate1 + here->JFETqgd) = qgga;
    *(ckt->CKTstate0 + here->JFETqgs) = *(ckt->CKTstate1 + here->JFETqgs) + 0.5 * (qgga-qggb + qggc-qggd);
    *(ckt->CKTstate0 + here->JFETqgd) = *(ckt->CKTstate1 + here->JFETqgd) + 0.5 * (qgga-qggc + qggb-qggd);
}
capgs = 0.5 * (cgsna + cgsnc);
capgd = 0.5 * (cgdna + cgdnb);
/* end Sydney University mod. */

/* Modification for Sydney University Universal JFET model
 * Copyright (c) January 1989 Anthony E. Parker & David J. Skellern
 * Laboratory for Communication Science Engineering
 * Sydney University Department of Electrical Engineering
 */

static double qggnew(vgs, vgd, phib, vcap2, vto, vmax, xc, cgs, cgd, *cgsnew, *cgdnew)
{
    double vgs, vgd, phib, vcap2, vto, vmax, xc, cgs, cgd, vnew1, ext;
    double qroot, qgval, par1, cfact, cplus, cminus, sqrt();
    veroot = sqrt( (vgs-vgd) * (vgs-vgd) + vcap2 );
    veff1 = 0.5 * (vgs + vgd + veroot);
    veff2 = veff1 - veroot;
    vnroot = (1-xc)*(veff1 - vto);
    vnroot = sqrt( vnroot*vnroot + 0.04 );
    vnew1 = 0.5 * ((1+xc)*veff1 + (1-xc)*vto + vnroot);
    if ( vnew1 < vmax ) {
        ext = 0;
        qroot = sqrt(1 - vnew1/phib);
        par1 = 0.5 * (1+xc + (1-xc)*(veff1-vto)/vnroot);
    } else {
        qroot = sqrt(1 - vmax/phib);
        ext = (vnew1-vmax)*(phib-1.5*vmax) + (vnew1*vnew1-vmax*vmax)/4)
        / (phib-vmax)/qroot;
        par1 = 0.25 * (1+xc + (1-xc)*(veff1-vto)/vnroot)
        (2*phib-3*vmax*vnew1)/(phib-vmax);
    }
    qgval = cgs * (2*phib*(1-qroot) + ext) + cgd*veff2;
    cfact = (vgs- vgd)/veroot;
    cplus = 0.5 * (1 + cfact);
    cminus = cplus - cfact;
    *cgsnew = cgs/qroot*par1*cplus + cgd*cminus;
    *cgdnew = cgs/qroot*par1*cminus + cgd*cplus;
    return(qgval);
}
/* end Sydney University mod. */
```
9.5 Numerical Calculations

9.5.1 Linear mode current

The standard Shockley FET equation can be approximated by using the Taylor expansion to give a polynomial expression as follows.

\[ I_d = q\mu N_d^2aL W_\infty \left( d^2 - s^2 - \frac{2}{3} (d^3 - s^3) \right) \]

\[ = q\mu N_d^2aL W_\infty \left( V_{ds} W_\infty - \frac{2}{3} \left( \frac{\phi_b - V_{gs} + V_{ds} - W_\infty}{W_\infty} \right)^{3/2} + \frac{2}{3} \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right)^{3/2} \right) \]

\[ = q\mu N_d^2aL W_\infty \left( V_{ds} W_\infty \frac{2}{3} \left( \frac{\phi_b - V_{gs} + V_{ds} - W_\infty}{W_\infty} \right)^{3/2} + \frac{2}{3} \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right)^{3/2} \right) \]

\[ = q\mu N_d^2aL W_\infty \left( \frac{V_{ds}}{W_\infty} \left( \frac{3\phi_b - V_{gs} - W_\infty}{W_\infty} + 3 \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right)^2 - \frac{1}{16} \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right)^3 \right) \right) \]

\[ = q\mu N_d^2aL W_\infty \left( \frac{1}{2} \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right) \right) \left( \frac{V_{ds}}{W_\infty} \right)^2 - \frac{1}{4} \left( \frac{V_{ds}}{W_\infty} \right)^2 \]

\[ + \frac{1}{8} \left( \frac{\phi_b - V_{gs} - W_\infty}{W_\infty} \right) \left( \frac{V_{ds}}{W_\infty} \right)^2 + \frac{1}{24} \left( \frac{V_{ds}}{W_\infty} \right)^3 \]

\[ I_d = q\mu N_d^2a \frac{V_{ds}}{3W_\infty L} \left[ B(2(V_{gs} + W_\infty - \phi_b) - V_{ds}) \right] \]

\[ + \frac{\phi}{W_\infty} \left[ V_{ds}^2 + 3(V_{gs} + W_\infty - \phi_b)(V_{gs} + W_\infty - \phi_b - V_{ds}) \right] \]  (9.1)

where \( B \) and \( \varphi \) can be adjusted to correct for the error in approximation. When \( V_{ds} = (V_{gs} + W_\infty - \phi_b) = W_\infty \), the term in braces, \( \{ \} \), should equal \( W_\infty \) which imposes the boundary condition \( B + \varphi = 1 \). The best least squares, and incidentally a very good fit to the original form, occurs when \( B = 0.6 \).
9.5.2 Onset of Velocity Saturation

The onset of velocity saturation occurs when the first region in Pucel’s analysis begins to occupy less than the whole channel length. In terms of Pucel’s notation this is equivalent to the condition \( L_1 = L \) and the relation between \( s \) and \( p \) is

\[
0 = \left( p^2 - s^2 - \frac{2}{3} \left( p^3 - s^3 \right) \right) - \xi (1-p) \quad (9-2)
\]

where

\[
p = \sqrt{\frac{\phi_b - V_{gs} + V_p}{W_{oo}}}.
\]

(9-3)

\( V_p \) is the potential of the channel relative to the source at the interface between the saturated and linear regions.

The term \((1-p)\) can be found by noting that the first derivative of equation (9-1) at \( V_p = 0 \) is the channel conductance given by

\[
\left. \frac{\partial I_d}{\partial V_p} \right|_{V_p=0} = \frac{\mu q N_d x_a}{L} (1-s) \quad (9-4)
\]

and so from equation (9-1) with \( \varphi = 1-B \),

\[
(1-s) = \frac{1}{3 W_{oo}} \left[ 2B (V_{gs} + W_{oo} - \phi_b) + (1-B) \frac{3}{W_{oo}} (V_{gs} + W_{oo} - \phi_b)^2 \right]. \quad (9-5)
\]

Substituting \( V_{gs} - \phi_b - V_p \) for \( V_{gs} - \phi_b \) gives

\[
(1-p) = \frac{1}{3 W_{oo}} \left[ 2B (V_{gs} + W_{oo} - \phi_b - V_p) + \frac{3(1-B)}{W_{oo}} (V_{gs} + W_{oo} - \phi_b - V_p)^2 \right]. \quad (9-6)
\]

Substituting this expression and (9-1) into (9-2) gives

\[
0 = V_p \left[ B (2(V_{gs} + W_{oo} - \phi_b) - V_p) + \frac{1-B}{W_{oo}} \left[ V_p^2 + 3 (V_{gs} + W_{oo} - \phi_b) (V_{gs} + W_{oo} - \phi_b) - V_p \right] \right] - \xi W_{oo} \left[ 2B (V_{gs} + W_{oo} - \phi_b - V_p) + \frac{3(1-B)}{W_{oo}} (V_{gs} + W_{oo} - \phi_b - V_p)^2 \right].
\]
Defining the right hand side as $f(V_p)$ gives the necessary condition at the onset of saturation

$$0 = f(V_p)$$

where

$$f(V_p) = \frac{(1-B)}{W_\infty} V_p^3 - \left[ \frac{3(1-B)}{W_\infty} (V_{gs} + W_\infty - \phi_h + \xi W_\infty) + B \right] V_p^2$$

$$+ \left[ 2B(V_{gs} + W_\infty - \phi_h + \xi W_\infty) + \frac{3(1-B)}{W_\infty} (V_{gs} + W_\infty - \phi_h) (V_{gs} + W_\infty - \phi_h + 2 \xi W_\infty) \right] V_p$$

$$- \xi W_\infty (V_{gs} + W_\infty - \phi_h) \left[ 2B + \frac{3(1-B)}{W_\infty} (V_{gs} + W_\infty - \phi_h) \right].$$

$f(x)$ is a cubic equation which has at least one root greater than zero. The minimum positive root can be found by the differential approximation

$$x \approx -\frac{2f(0)}{f'(0) + f'(x)}$$

$$\approx -\frac{2f(0)}{f'(0) + f'\left(\frac{2f(0)}{f'(0)}\right)}$$

$$\approx \frac{\xi W_\infty (V_{gs} + W_\infty - \phi_h)}{V_{gs} + W_\infty - \phi_h + \xi W_\infty - \frac{B \xi W_\infty^2 (V_{gs} + W_\infty - \phi_h)}{(V_{gs} + W_\infty - \phi_h + \xi W_\infty) (2W_\infty B + 3(1-B) (V_{gs} + W_\infty - \phi_h))}}$$

$$\approx \frac{\xi W_\infty (V_{gs} + W_\infty - \phi_h)}{V_{gs} + W_\infty - \phi_h + \xi W_\infty}$$

This root corresponds with the value of $V_{ds}$ at the onset of velocity saturation.
### 9.6 Properties of Semiconductors

Table 9.9. Properties of Semiconductors at 300 K after [Sze 1985]

<table>
<thead>
<tr>
<th>Property</th>
<th>Ge</th>
<th>Si</th>
<th>GaAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic Density (Atoms/cm$^3$)</td>
<td>4.42×10$^{22}$</td>
<td>5.0×10$^{22}$</td>
<td>2.21×10$^{22}$</td>
</tr>
<tr>
<td>Atomic Weight</td>
<td>72.6</td>
<td>28.09</td>
<td>144.63</td>
</tr>
<tr>
<td>Breakdown Field (V/cm)</td>
<td>=10$^5$</td>
<td>=3×10$^5$</td>
<td>=4×10$^5$</td>
</tr>
<tr>
<td>Crystal Structure</td>
<td>Diamond</td>
<td>Diamond</td>
<td>Zincblende</td>
</tr>
<tr>
<td>Density (g/cm$^3$)</td>
<td>5.3267</td>
<td>2.328</td>
<td>5.32</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effective Density of States</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>in Conduction Band $N_C$ (cm$^{-3}$)</td>
<td>1.04×10$^{19}$</td>
<td>2.8×10$^{19}$</td>
<td>4.7×10$^{17}$</td>
</tr>
<tr>
<td>in Valence Band $N_V$ (cm$^{-3}$)</td>
<td>6.0×10$^{18}$</td>
<td>1.04×10$^{19}$</td>
<td>7.0×10$^{18}$</td>
</tr>
<tr>
<td>Effective Mass</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electron ($m_e^*/m_o$)</td>
<td>1.64</td>
<td>0.98</td>
<td>0.067</td>
</tr>
<tr>
<td>Electron ($m_t^*/m_o$)</td>
<td>0.082</td>
<td>0.19</td>
<td>-</td>
</tr>
<tr>
<td>Electron ($m_h^*/m_o$)</td>
<td>-</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>Hole ($m_e^*/m_o$)</td>
<td>0.044</td>
<td>0.16</td>
<td>0.082</td>
</tr>
<tr>
<td>Hole ($m_t^*/m_o$)</td>
<td>0.28</td>
<td>0.49</td>
<td>0.45</td>
</tr>
<tr>
<td>Electron Affinity, $\chi$ (V)</td>
<td>4.0</td>
<td>4.05</td>
<td>4.07</td>
</tr>
<tr>
<td>Energy Gap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0K (V)</td>
<td>0.74</td>
<td>1.17</td>
<td>1.52</td>
</tr>
<tr>
<td>300K (V)</td>
<td>0.66</td>
<td>1.12</td>
<td>1.424</td>
</tr>
<tr>
<td>Intrinsic Carrier Conc (cm$^{-3}$)</td>
<td>2.4×10$^{13}$</td>
<td>1.45×10$^{10}$</td>
<td>1.79×10$^{6}$</td>
</tr>
<tr>
<td>Lattice Constant (Å)</td>
<td>5.64613</td>
<td>5.43095</td>
<td>5.6533</td>
</tr>
<tr>
<td>Linear Coefficient of Thermal Expansion $\Delta L/L\Delta T$ (°C)</td>
<td>5.8×10$^{-6}$</td>
<td>2.6×10$^{-6}$</td>
<td>6.86×10$^{-6}$</td>
</tr>
<tr>
<td>Mean Free Path $l_o$ (Å)</td>
<td>105±10</td>
<td>75±5</td>
<td>58±5</td>
</tr>
<tr>
<td>Melting Point (°C)</td>
<td>937</td>
<td>1415</td>
<td>1238</td>
</tr>
<tr>
<td>Minority Carrier Lifetime (sec)</td>
<td>10$^{-3}$</td>
<td>2.5×10$^{-3}$</td>
<td>10$^{-8}$</td>
</tr>
<tr>
<td>Mobility Electron (cm$^2$/Vs)</td>
<td>3900</td>
<td>1500</td>
<td>8500</td>
</tr>
<tr>
<td>@ $N_d$=10$^{23}$</td>
<td>1000</td>
<td>5000</td>
<td></td>
</tr>
<tr>
<td>Hole (cm$^2$/Vs)</td>
<td>1900</td>
<td>450</td>
<td>400</td>
</tr>
<tr>
<td>@ $N_d$=10$^{23}$</td>
<td>350</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>Optical Phonon Energy $E_p$ (eV)</td>
<td>0.037</td>
<td>0.063</td>
<td>0.035</td>
</tr>
<tr>
<td>Specific Heat (J/g/°C)</td>
<td>0.31</td>
<td>0.7</td>
<td>0.35</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm/°C)</td>
<td>0.64</td>
<td>1.45</td>
<td>0.46</td>
</tr>
<tr>
<td>Thermal Diffusivity (cm$^2$/sec)</td>
<td>0.36</td>
<td>0.9</td>
<td>0.24</td>
</tr>
<tr>
<td>Work Function (eV)</td>
<td>4.4</td>
<td>4.8</td>
<td>4.7</td>
</tr>
</tbody>
</table>
Text Books


Review Papers


Chapter 10: Categorized Reference List


Reported Applications


**Reported Developments in Logic Topology**


Chapter 10: Categorized Reference List


**Devices**


**Device Models**


**Models of Specific Phenomenon**


**Parasitic Elements**


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*IEEE J. of Solid-State Circuits*, vol. 17, no. 6, pp. 1226-1231, 1982],
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*Memorandum No. UCB/ERL M89/46*, Electronics Research Laboratory, College of Engineering, University of California, Berkeley, 24 April 1989.

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**Data**


